Sixteen (16) LVDT Measurement Channels

2-Wire or 3/4-Wire LVDT to Digital Converters
Auto-ranging; Optional On-Board Excitation
FOR COMMERCIAL AND MILITARY APPLICATIONS

- 16-bit resolution
- 0.025% FS accuracy
- Continuous background BIT testing with Excitation and Signal loss detection
- **Self-calibrating. Does not require removal for calibration**
- 360 Hz to 10 kHz operation
- Auto-ranging input between 2.0 and 28 Vrms
- 12, 8 and 4-channel versions available
- Optional programmable reference excitation
- Transformer isolated
- LATCH feature
- Geographical Addressing
- Compensates for ±60° phase shift
- I/O via front panel, P2 or both
- No adjustments or trimming required
- Optional programmable encoder (A & B) plus index outputs
- Part number, S/N, Date Code, and Revision in non-volatile memory

DESCRIPTION:

This high-density intelligent DSP-based card incorporates up to sixteen (16) separate transformer isolated programmable LVDT/RVDT-to-Digital tracking converters with extensive diagnostics, and optional programmable excitation supply. Instead of buying cards that are set for specific inputs, the uniqueness of this design makes it possible to order our standard card that auto ranges between 2.0 and 28 volts. Operating frequency between 400 Hz and 10 kHz can be specified (see part number). This card can be used for 4-wire or 3-wire LVDT inputs. The output is computed as A-B/A+B and is expressed as %FS. This card uses a derived reference ratio-metric design approach that is insensitive to magnitude, temperature, frequency and phase shift effects. The ratio-metric technique assures that the output will change only when the LVDT position changes and will ignore excitation voltage variations. The LATCH feature permits the user to read all channels at the same time. Reading will unlatch that channel. The converters utilize a Type II servo loop processing technique that enables tracking, at full accuracy, up to the specified rate. Intermediate transparent latches, on all data outputs, guarantee that current valid data is always available for any channel without affecting the tracking performance of the converters. No interrupts or waiting time are required. Each channel also produces differential (A & B) incremental encoder outputs (with programmable resolution) and a zero degree marker pulse. If Geographical Addressing is enabled, the board DIP switches will be automatically deactivated. The optional on–board excitation is field programmable. To simplify logistics, Part Number, S/N, Date Code, and Revision are stored in non-volatile memory locations.

This board incorporates major diagnostics that offer substantial improvements to system reliability because the user is alerted to channel malfunction. This approach reduces bus traffic, because the Status Registers need not be constantly polled. Three different tests (one on-line and two off-line) can be selected**,**

The D2 Test initiates automatic background BIT testing. Each channel is checked over the programmed signal range to a measuring accuracy 0.1% FS, and each Signal and Excitation is monitored. Any failure triggers an Interrupt (if enabled) and the results are available in registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 Test, if enabled, starts an initiated BIT Test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and measures multiple voltages to a test accuracy of 0.1%FS. External excitation is not required. Any failure triggers an interrupt (if enabled) and results can be read from registers. The testing requires no external programming and can be initiated or terminated via the bus.

Power-On Self-Test (POST): when enabled and saved, will initiate the D3 Test upon Power-On

The D0 Test is used to check the card and the VME interface. All channels are disconnected from the outside world, allowing user to write any number of input positions to the card and then read the data from the interface. External excitation is not required.

SPECIFICATIONS:	(applies to each channel)
Number of channels:	4, 8, 12 or 16 (see part number)
Resolution:	16-bit
Accuracy:	0.025% FS
Bandwidth:	10% of excitation to 100 Hz max. BW and tracking rate can easily be customized**.**
Input format:	LVDT or RVDT
Input voltage	Auto-ranging from 2.0 to 28 Vrms. Transformer isolated.
Excitation voltage:	Not required for computation of output but should be connected to allow card to check for excitation loss.
Input Impedance:	40 kΩ min. at 360 Hz
Frequency:	Specify between 360 Hz to 10 kHz, (See Part Number and Code Table)
Encoder outputs:	Either 12,13,14,15, or 16-bit resolution, (field programmable) and Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N).
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and Output up to ±60° (3-wire units ignore phase shift)
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.
Base address:	Responds to Geographical Addressing. Otherwise, the board DIP switches are activated for setting base address to A32, A24 or A16.
VME Data transfer:	Data transfers within 200 ns.
Interrupts:	One –Interrupt capability is implemented. One of seven priority lines can be specified.
Power:	+ 5 VDC at 0.35 A ±12 VDC at 0.1 A without Excitation; 1.1 A for 5 VA Excitation Output
Temperature, operating:	"C"=0°C to +70°C; "e"= -40°C to +85°C. (See part number)
Storage temperature:	-55°C to +105°C.
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	20 oz.
REFERENCE SUPPLY:	Optional. (See part number).
Voltage:	2-28Vrms programmable, or 115 Vrms fixed. Resolution 0.1 Vrms, Accuracy ±2%
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 190mA RMS @ 2-28VAC, 45mA RMS @ 115VAC Note: Power is reduced linearly as the Reference Voltage decreases (2-28VRMS): i.e. Up 190mA can be delivered to a load for that respective reference voltage range.

Principals of LVDT Operation: Typically the LVDT primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

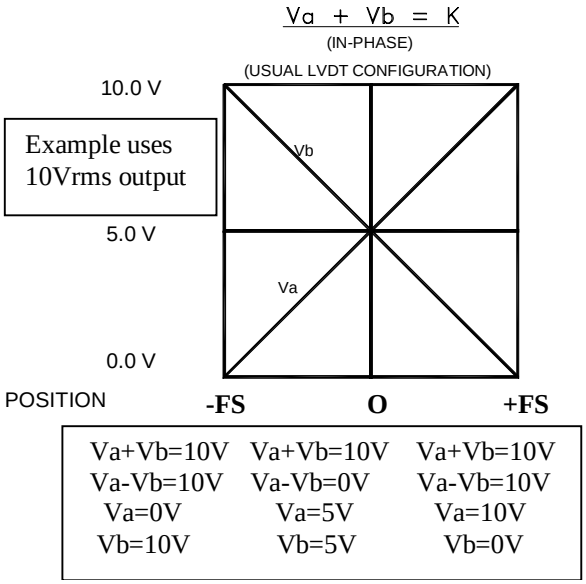
Interfacing the LVDT to the Converter: Two common connection methods are:

Primary as reference (two-wire system)
This method of connection converts the widest range of LVDT sensors and is the most sensitive to excitation voltage variations, temperature and phase shift effects.

Derived reference (three/four-wire LVDT)

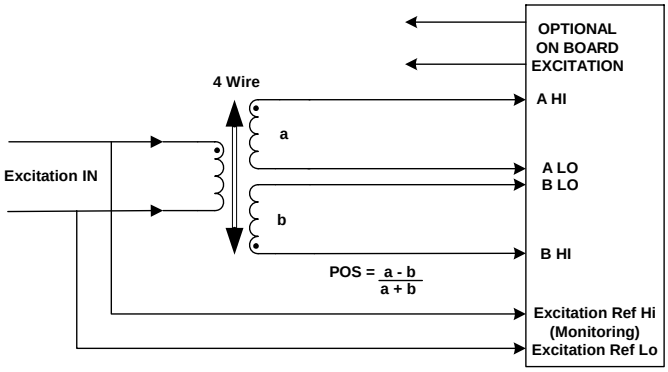
The LVDT is again excited from the primary side, but the converter reference is the sum of A + B that has constant amplitude for changing core displacement. This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity (A-B)/(A+B)

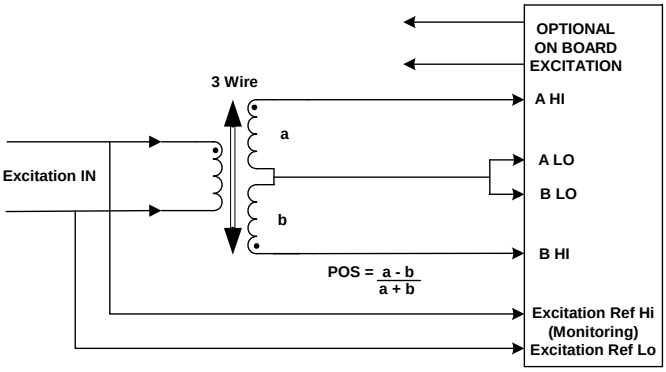
LVDT Coil Voltage vs. Position

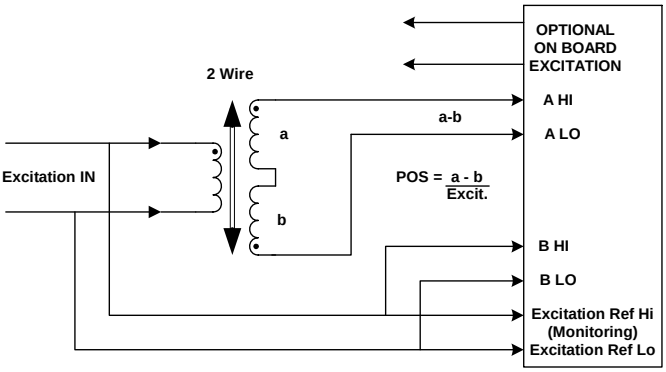


Va+Vb=10V	Va+Vb=10V	Va+Vb=10V
Va-Vb=10V	Va-Vb=0V	Va-Vb=10V
Va=0V	Va=5V	Va=10V
Vb=10V	Vb=5V	Vb=0V

Various LVDT configurations







LVDT Connections:

For 3,4 Wire LVDT's, connect A and B LVDT outputs to Signal A and B inputs. Excitation is not used, but should be connected to allow card to monitor and report any excitation loss.

For 2 Wire LVDT's, connect A-B output of LVDT to card "A" input and connect external excitation voltage to card "B" input and to excitation input to allow card to monitor and report any excitation loss.

PROGRAMMING INSTRUCTIONS:

I/O CONFIGURATION:
The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 512 byte boundaries.

A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 512 byte boundaries.

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 512 byte boundaries.

Note: Address switch A8 must be set to "ON" (logic 0*)* for 512 byte boundaries.

Enable Geographical Addressing by removing jumper from JP2. Disable Geographical Addressing by adding jumper to JP2.

Geographical Addressing: When Geographical Addressing is enabled, the card will respond to address modifier 2Fh for A24 Address mode, where the 5 MSBs of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:
1) the base address of the card should respond to,
2) the address modifier (A16, A24, A32),
3) then, enable the card.

For example: If the card is in slot # 10 the 5 MSBs are 01010 so the address of the CSR Registers are:
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)
Write to address 57FF63 h, the A31 – A24 base address bits , for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h, the address modifier you wish to respond to shifted up 2 bits;
For example, 28h(0A<< 2)

Then, Write to address 57FFFBh , 10h to enable the card.

The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

MEMORY MAP

000	Data Ch. 1	read	052	Scale, Ch. 10	read/write	0CE	Velocity, scale Ch. 8	read/write
002	Data Ch. 2	read	054	Scale, Ch. 11	read/write	0D0	Velocity, scale Ch. 9	read/write
004	Data Ch. 3	read	056	Scale, Ch. 12	read/write	0D2	Velocity, scale Ch. 10	read/write
006	Data Ch. 4	read	058	Scale, Ch. 13	read/write	0D4	Velocity, scale Ch. 11	read/write
008	Data Ch. 5	read	05A	Scale, Ch. 14	read/write	0D6	Velocity, scale Ch. 12	read/write
00A	Data Ch. 6	read	05C	Scale, Ch. 15	read/write	0D8	Velocity, scale Ch. 13	read/write
00C	Data Ch. 7	read	05E	Scale, Ch. 16	read/write	0DA	Velocity, scale Ch. 14	read/write
00E	Data Ch. 8	read	072	Active Channels	read/write	0DC	Velocity, scale Ch. 15	read/write
010	Data Ch. 9	read	074	Test D2 Verify	read/write	0DE	Velocity, scale Ch. 16	read/write
012	Data Ch. 10	read	076	Test Enable	read/write	0E0	Magnitude (A+B) Ch. 1	read
014	Data Ch. 11	read	078	Status, Signal	read	0E2	Magnitude (A+B) Ch. 2	read
016	Data Ch. 12	read	07A	Status, Excitation	read	0E4	Magnitude (A+B) Ch. 3	read
018	Data Ch. 13	read	07C	Status, Test	read	0E6	Magnitude (A+B) Ch. 4	read
01A	Data Ch. 14	read	07E	Latch	write	0E8	Magnitude (A+B) Ch. 5	read
01C	Data Ch. 15	read	080	LVDT/D Test Position	read/write	0EA	Magnitude (A+B) Ch. 6	read
01E	Data Ch. 16	read	084	Interrrupt Vector 1(failure)	read/write	0EC	Magnitude (A+B) Ch. 7	read
020	Velocity, Ch. 1	read	088	2-3/4 Wire Mode	read/write	0EE	Magnitude (A+B) Ch. 8	Read
022	Velocity, Ch. 2	read	08A	Power-On (POST) Enable	read/write	0F0	Magnitude (A+B) Ch. 9	Read
024	Velocity, Ch. 3	read	0A0	(A&B) resolution Ch. 1	read/write	0F2	Magnitude (A+B) Ch. 10	Read
026	Velocity, Ch. 4	read	0A2	(A&B) resolution Ch. 2	read/write	0F4	Magnitude (A+B) Ch. 11	Read
028	Velocity, Ch. 5	read	0A4	(A&B) resolution Ch. 3	read/write	0F6	Magnitude (A+B) Ch. 12	Read
02A	Velocity, Ch. 6	read	0A6	(A&B) resolution Ch. 4	read/write	0F8	Magnitude (A+B) Ch. 13	Read
02C	Velocity, Ch. 7	read	0A8	(A&B) resolution Ch. 5	read/write	0FA	Magnitude (A+B) Ch. 14	read
02E	Velocity, Ch. 8	read	0AA	(A&B) resolution Ch. 6	read/write	0FC	Magnitude (A+B) Ch. 15	read
030	Velocity, Ch. 9	read	0AC	(A&B) resolution Ch. 7	read/write	0FE	Magnitude (A+B) Ch. 16	read
032	Velocity, Ch. 10	read	0AE	(A&B) resolution Ch. 8	read/write	100	Internal Excitation Freq.	read/write
034	Velocity, Ch. 11	read	0B0	(A&B) resolution Ch. 9	read/write	102	Internal Excitation Eo	read/write
036	Velocity, Ch. 12	read	0B2	(A&B) resolution Ch. 10	read/write	104	Watchdog Timer	read/write
038	Velocity, Ch. 13	read	0B4	(A&B) resolution Ch. 11	read/write	106	Soft Reset	write
03A	Velocity, Ch. 14	read	0B6	(A&B) resolution Ch. 12	read/write	108	Interrupt Level	read/write
03C	Velocity, Ch. 15	read	0B8	(A&B) resolution Ch. 13	read/write	10A	Part #	read
03E	Velocity, Ch. 16	read	0BA	(A&B) resolution Ch. 14	read/write	10C	Serial #	read
040	Scale, Ch. 1	read/write	0BC	(A&B) resolution Ch. 15	read/write	10E	Date Code	read
042	Scale, Ch. 2	read/write	0BE	(A&B) resolution Ch. 16	read/write	110	Rev PCB	read
044	Scale, Ch. 3	read/write	0C0	Velocity, scale Ch. 1	read/write	112	Rev Master uP	read
046	Scale, Ch. 4	read/write	0C2	Velocity, scale Ch. 2	read/write	114	Rev Master FPGA	read
048	Scale, Ch. 5	read/write	0C4	Velocity, scale Ch. 3	read/write	116	Rev Slave uP	read
04A	Scale, Ch. 6	read/write	0C6	Velocity, scale Ch. 4	read/write	118	Rev Slave FPGA	read
04C	Scale, Ch. 7	read/write	0C8	Velocity, scale Ch. 5	read/write	11A	Rev Interface FPGA	read
04E	Scale, Ch. 8	read/write	0CA	Velocity, scale Ch. 6	read/write	11C	Save	read/write
050	Scale, Ch. 9	read/write	0CC	Velocity, scale Ch. 7	read/write			

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Latch Outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Active channels	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Status, Test	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Status, Signal	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Status, Excitation	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
2 or 3,4 wire Input	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
(A & B) resolution	0	X	X	X	X	X	X	X	X	X	X	X	X	**D2**	**D1**	**D0**
												16 bit		0	0	0
												15 bit		0	0	1
												14 bit		0	1	0
												13 bit		0	1	1
												12 bit		1	0	0

(A & B) resolution: ↑

PROGRAMMING INSTRUCTIONS:

Irrespective of the method of connection, the codes will be 2's complement.
At **Power-On** or **System Reset**, all parameters are restored to last saved setup.

Enter Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the *Active Channel Register*. "1"=active; "0"=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: Writing 5555h to the *Save Register* can save the current setup. This location will automatically clear to 0000h when the save is completed (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up.

To restore factory shipped parameters, write AAAAh to the *Save Register* followed by System Reset. Note**:** After a SAVE or RESTORE, poll the *Save Register* and do not perform any other operation until word is at "0".

Optional Reference/Excitation Supply: For excitation frequency, write a 16-bit word (Ex: 400 Hz = 110010000) to the *Internal Excitation Frequency Register*. For voltage, write an 16-bit word (Ex: 26.1Vrms =100000101) with LSB=0.1Vrms, to *Internal Excitation Eo Register*. It is recommended that user program the required frequency before setting the output voltage.

Interrupt Level: Enter interrupt level in the *Interrupt Level Register* as a 16-bit binary number.
0 = no interrupt; 1-7 indicates priority levels.

Interrupt Vector 1: Enter interrupt service address in *Interrupt Vector 1 Register* for failure reports. Address range is from 0 to 255 (0x0000 to 0x00FF).

Selecting 2 or 3,4 Wire operation: Program the corresponding bit for the appropriate channel in the *2-3/4 Wire Register*. Logic 1 = 2 wire; Logic 0 = 3 or 4 wire.

Data Format:

For 4-wire or 3-wire inputs, the output data is A-B/A+B and represents %FS. Format is two's complement. Maximum positive excursion is 32767 (7FFFh), 0 = 0, and maximum negative excursion is -32768 (8000h).

For 2-wire input, the output data is A-B/Excitation and represents %FS. Format is two's complement. Maximum positive excursion is 32767 (7FFFh), 0 = 0, and maximum negative excursion is -32768 (8000h).

Programming Scale Registers

The 4-wire or 3-wire LVDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs, no scaling is required because the inputs are auto-ranging, however the corresponding *Scale Register* can be used to scale the output code.

Default settings for the *Scale Registers* are set to 65535 (FFFFh) which results in a full-scale output reading for full travel of the LVDT. A full-scale output reading for less than full travel of the LVDT can be obtained by writing a scale value to the corresponding *Scale Register*. For example, writing 32768 (8000h) to *Scale Ch. 1 Register* will result in channel 1 having a full-scale output reading for one-half travel of the LVDT.

For 2-wire input, the default settings for the *Scale Registers* are 65535 (FFFFh), which result in a full-scale output reading for full travel of the LVDT for TR = 1 (transformer ratio). To achieve full output readings for TR < 1, a scale factor (SF) should be programmed into the corresponding *Scale Register*. This is calculated from the equation:
SF =65535 (FFFFh) x TR

The calculated SF value is written to the corresponding *Scale Register.*

Read (A+B): Read binary number from the *(A+B) Magnitude Register* and multiply by 0.01 Volt. Only valid for 3 or 4 wire configurations.

Velocity Scale Factor: To scale the Max Velocity word for 152.5878 Strokes / Second (SPS), set Velocity Scale Factor = 4095 in HEX (max velocity word of 7FFFh being max. CW rotation, and 8000h being max. CCW rotation).
Scaling effects **only** the Velocity output word and not the dynamic performance.

Ex: To get max. velocity word @ 152.5878 SPS: 4095(152.5878/152.5878) = 4095 (0FFFh), also the Factory setting.
To get max. velocity word @ 50.8626 SPS: 4095(152.5875/50.8626) = 12,285 (2FFDh)
To get max. velocity word @ 9.5367 SPS: 4095(152.5878/9.5367) = 65,520 (FFF0h), also the lowest setting.

Velocity Output: Read Velocity registers of each channel as a 2's complement word, with 7FFFh being max. CW rotation, and 8000h being max. CCW rotation.

When max. velocity is set to 152.5878 SPS, an actual speed of 10 SPS CW would be read as 0863h.
When max. velocity is set to 152.5878 SPS, an actual speed of 10 SPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 SPS, an actual speed of 10 SPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 SPS, an actual speed of 10 SPS CCW would be read as E6D5h.

To convert a velocity word, for example E6D5h, into sps: If max. velocity set to 50.8626 SPS, then
SPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 SPS

Latch: All channels may be latched by writing a "1" to D1 in the *Latch Register*. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

D2 Test Enable: Writing a "1" to the D2 bit of the *Test Enable Register* initiates automatic background BIT testing. Each channel is checked over the programmed Signal range to a measuring accuracy 0.1%FS. An Interrupt will be set to indicate an accuracy problem. A "0" deactivates this test The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. The results are available in Test Status Registers. The card will write 55h to the *Test D2 Verify Register* when D2 Test is enabled. User can periodically clear to 00h and then read the *Test D2 Verify Register* again, after 30 seconds, to verify that background BIT testing is activated.

In addition, each Signal and Excitation input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and Excitation *Status Registers*.

Status, Test: Check the corresponding bit of the *Test Status Register*, for status of BIT testing for each active channel. A "1" =Accuracy OK; "0" = failed. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the Test Status Register. Reading will unlatch register.

Status, Excitation: Check the channel's corresponding bit of the *Excitation Status Register*, for status of the Excitation input for each active channel. A "1" = Excitation. ON, "0" = Excitation. Loss. Channels that are inactive are also set to "0". (Excitation loss is detected after 2 seconds). Excitation monitoring is disabled during D3 or D0 Test. Any Excitation status failure, transient or intermittent will latch the Excitation *Status Register*. Reading will unlatch register.

Status, Signal: Check the channel's corresponding bit of the *Signal Status Register*, for status of the input signals for each active channel. A "1" = Signal ON, "0" = Signal loss. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

D3 Test Enable: Power-on Self-Test (POST), if enabled, or writing a "1" to D3 in the *Test Enable Register*, starts an initiated BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates multiple test voltages that are measured to a test accuracy of 0.1%FS. Test cycle takes about 10 seconds and results can be read from the Test Status Register when D3 changes from "1" to "0". External excitation is not required. An Interrupt, if enabled will be generated if a BIT failure is detected (See *Interrupt Register*). Testing requires no external programming and can be terminated by writing "0" to D3 of the *Test Enable Register*.

Signal and Excitation monitoring is disabled during D3 test.

D0 Test Enable: Checks the card and the VME interface. Writing a "1" to D0 in the *Test Enable Register* disconnects all channels from the outside world, allowing user to write any number of input positions to the card in the *LVDT/D Test Position Register* and then reads the data from the VME interface (allow 50 ms after writing). External excitation is not required.

Signal and Excitation monitoring is disabled during D0 test.

(A&B) Encoder Resolution: Enter required resolution, for each channel, per above table (Register Bit Map). Can be changed on the fly. Encoder outputs are optional, see part ordering information. Default is 12 bit encoder output.

Watchdog Timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec, should look for the inverted code to confirm that the processor is operating.

Soft Reset: (Level sensitive): Writing a "1" to the *Soft Reset Register* initiates and holds software in reset state. Then, writing "0" initiates reboot (takes 400 ms). This function is equivalent to a power-on reset

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: Read as a 16 bit binary word from the *Serial Number Register*. This is the serial number of that

particular board.

Date Code: Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week).

Rev Levels: There are a total of 6 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Rev level PCB
Rev level Master DSP
Rev level Master FPGA
Rev level Slave DSP
Rev level Slave FPGA
Rev level Interface FPGA

VME64LD2 Connector Information

Front panel Connectors (78 PIN) Amp 748483, Mating Connector Adamtec HDT78PD

Slot 1		Slot 2		Slot 4		Slot 5	
Pin #	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**
J1- 1	SIG A LO CH1	J1- 27	SIG A LO CH5	J2- 1	SIG A LO CH9	J2- 27	SIG A LO CH13
J1- 21	SIG A HI CH1	J1- 8	SIG A HI CH5	J2- 21	SIG A HI CH9	J2- 8	SIG A HI CH13
J1- 2	SIG B HI CH1	J1- 28	SIG B HI CH5	J2- 2	SIG B HI CH9	J2- 28	SIG B HI CH13
J1- 22	SIG B LO CH1	J1- 9	SIG B LO CH5	J2- 22	SIG B LO CH9	J2- 9	SIG B LO CH13
J1- 3	Exc. HI CH1	J1- 29	Exc. HI CH5	J2- 3	Exc. HI CH9	J2- 29	Exc. HI CH13
J1- 23	Exc.LO CH1	J1- 10	Exc.LO CH5	J2- 23	Exc. LO CH9	J2- 10	Exc.LO CH13
J1- 4	SIG A LO CH2	J1- 30	SIG A LO CH6	J2- 4	SIG A LO CH10	J2- 30	SIG A LO CH14
J1- 24	SIG A HI CH2	J1- 11	SIG A HI CH6	J2- 24	SIG A HI CH10	J2- 11	SIG A HI CH14
J1- 5	SIG B HI CH2	J1- 31	SIG B HI CH6	J2- 5	SIG B HI CH10	J2- 31	SIG B HI CH14
J1- 25	SIG B LO CH2	J1- 12	SIG B LO CH6	J2- 25	SIG B LO CH10	J2- 12	SIG B LO CH14
J1- 6	Exc. HI CH2	J1- 32	Exc. HI CH6	J2- 6	Exc. HI CH10	J2- 32	Exc. HI CH14
J1- 26	Exc. LO CH2	J1- 13	Exc. LO CH6	J2- 26	Exc. LO CH10	J2- 13	Exc. LO CH14
J1- 40	SIG A LO CH3	J1- 66	SIG A LO CH7	J2- 40	SIG A LO CH11	J2- 66	SIG A LO CH15
J1- 60	SIG A HI CH3	J1- 47	SIG A HI CH7	J2- 60	SIG A HI CH11	J2- 47	SIG A HI CH15
J1- 41	SIG B HI CH3	J1- 67	SIG B HI CH7	J2- 41	SIG B HI CH11	J2- 67	SIG B HI CH15
J1- 61	SIG B LO CH3	J1- 48	SIG B LO CH7	J2- 61	SIG B LO CH11	J2- 48	SIG B LO CH15
J1- 42	Exc. HI CH3	J1- 68	Exc. HI CH7	J2- 42	Exc. HI CH11	J2- 68	Exc. HI CH15
J1- 62	Exc. LO CH3	J1- 49	Exc. LO CH7	J2- 62	Exc. LO CH11	J2- 49	Exc. LO CH15
J1- 43	SIG A LO CH4	J1- 69	SIG A LO CH8	J2- 43	SIG A LO CH12	J2- 69	SIG A LO CH16
J1- 63	SIG A HI CH4	J1- 50	SIG A HI CH8	J2- 63	SIG A HI CH12	J2- 50	SIG A HI CH16
J1- 44	SIG B HI CH4	J1- 70	SIG B HI CH8	J2- 44	SIG B HI CH12	J2- 70	SIG B HI CH16
J1- 64	SIG B LO CH4	J1- 51	SIG B LO CH8	J2- 64	SIG B LO CH12	J2- 51	SIG B LO CH16
J1- 45	Exc. HI CH4	J1- 71	Exc. HI CH8	J2- 45	Exc. HI CH12	J2- 71	Exc. HI CH16
J1- 65	Exc. LO CH4	J1- 52	Exc. LO CH8	J2- 65	Exc. LO CH12	J2- 52	Exc. LO CH16
				J2- 33	Exc. HI – OUT	J2- 72	Exc. LO – OUT

Note: Do not connect to any unspecified pins

Rear Connector

P2E		P2A		P2C		P2D	
Pin #	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**	**Pin #**	**Signal Name**
1 Z	Not used	1 A	SIG B HI CH10	1 C	Exc. HI CH11	1 D	Exc. HI CH13
2 Z	Not used	2 A	SIG B LO CH10	2 C	Exc. LO CH11	2 D	Exc.LO CH13
3 Z	Not used	3 A	SIG A LO CH11	3 C	SIG A LO CH12	3 D	SIG A LO CH14
4 Z	Not used	4 A	SIG A HI CH11	4 C	SIG A HI CH12	4 D	SIG A HI CH14
5 Z	Not used	5 A	SIG B HI CH11	5 C	SIG B HI CH12	5 D	SIG B HI CH14
6 Z	Not used	6 A	SIG B LO CH11	6 C	SIG B LO CH12	6 D	SIG B LO CH14
7 Z	Not used	7 A	SIG A LO CH13	7 C	SIG A HI CH13	7 D	SIG A LO CH15
8 Z	Not used	8 A	SIG A LO CH4	8 C	SIG B HI CH7	8 D	SIG A HI CH15
9 Z	Not used	9 A	SIG A HI CH4	9 C	SIG B LO CH7	9 D	SIG B HI CH15
10 Z	Not used	10 A	SIG B HI CH4	10 C	Exc. HI CH7	10 D	SIG B LO CH15
11 Z	Not used	11 A	SIG B LO CH4	11 C	Exc. LO CH7	11 D	Exc. HI CH15
12 Z	Not used	12 A	SIG A LO CH5	12 C	SIG A LO CH8	12 D	Exc. LO CH15
13 Z	Not used	13 A	SIG A HI CH5	13 C	SIG A HI CH8	13 D	SIG A LO CH16
14 Z	Not used	14 A	SIG B HI CH5	14 C	SIG B HI CH8	14 D	SIG A HI CH16
15 Z	Not used	15 A	SIG B LO CH5	15 C	SIG B LO CH8	15 D	SIG B HI CH16
16 Z	Not used	16 A	Exc. HI CH5	16 C	SIG A LO CH9	16 D	SIG B LO CH16
17 Z	Not used	17 A	Exc.LO CH5	17 C	SIG A HI CH9	17 D	Exc. HI CH2
18 Z	Not used	18 A	SIG A LO CH6	18 C	SIG B HI CH9	18 D	Exc. LO CH2
19 Z	Not used	19 A	SIG A HI CH6	19 C	SIG B LO CH9	19 D	Exc. HI CH4
20 Z	Not used	20 A	SIG B HI CH6	20 C	Exc. HI CH9	20 D	Exc. LO CH4
21 Z	Not used	21 A	SIG B LO CH6	21 C	Exc.LO CH9	21 D	Exc. HI CH6
22 Z	Not used	22 A	SIG B HI CH13	22 C	SIG B LO CH13	22 D	Exc. LO CH6
23 Z	Not used	23 A	SIG A LO CH7	23 C	SIG A LO CH10	23 D	Exc. HI CH8
24 Z	Not used	24 A	SIG A HI CH7	24 C	SIG A HI CH10	24 D	Exc. LO CH8
25 Z	Exc HI-OUT	25 A	SIG A LO CH1	25 C	SIG B HI CH2	25 D	Exc. HI CH10
26 Z	Not used	26 A	SIG A HI CH1	26 C	SIG B LO CH2	26 D	Exc. LO CH10
27 Z	Exc LO-OUT	27 A	SIG B HI CH1	27 C	SIG A LO CH3	27 D	Exc. HI CH12
28 Z	Not used	28 A	SIG B LO CH1	28 C	SIG A HI CH3	28 D	Exc. LO CH12
29 Z	Exc. HI CH16	29 A	Exc. HI CH1	29 C	SIG B HI CH3	29 D	Exc. HI CH14
30 Z	Not used	30 A	Exc.LO CH1	30 C	SIG B LO CH3	30 D	Exc. LO CH14
31 Z	Exc. LO CH16	31 A	SIG A LO CH2	31 C	Exc. HI CH3	31 D	Not used
32 Z	Not used	32 A	SIG A HI CH2	32 C	Exc. LO CH3	32 D	Not used

Note: Do not connect to any unspecified pins

P0 Connector Encoder outputs (Optional)									
P0 A		P0 B		P0 C		P0 D		P0 E	
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
A 1	ENC A HI CH9	B 1	ENC A HI CH10	C 1	IDX HI CH10	D 1	ENC A HI CH11	E 1	ENC A HI CH12
A 2	ENC A LO CH9	B 2	ENC A LO CH10	C 2	IDX LO CH10	D 2	ENC A LO CH11	E 2	ENC A LO CH12
A 3	ENC B HI CH9	B 3	ENC B HI CH10	C 3	IDX HI CH12	D 3	ENC B HI CH11	E 3	ENC B HI CH12
A 4	ENC B LO CH9	B 4	ENC B LO CH10	C 4	IDX LO CH12	D 4	ENC B LO CH11	E 4	ENC B LO CH12
A 5	IDX HI CH9	B 5	IDX LO CH9	C 8	ENC A LO CH1	D 5	IDX HI CH11	E 5	IDX LO CH11
A 8	Not used	B 8	ENC A HI CH1	C 9	ENC A HI CH2	D 8	ENC B HI CH1	E 8	ENC B LO CH1
A 9	Not used	B 9	ENC A LO CH2	C 10	ENC B LO CH2	D 9	IDX LO CH1	E 9	IDX HI CH1
A 10	Not used	B 10	ENC B HI CH2	C 11	ENC B HI CH3	D 10	IDX HI CH2	E 10	IDX LO CH2
A 11	Not used	B 11	ENC B LO CH3	C 12	IDX LO CH3	D 11	ENC A LO CH3	E 11	ENC A HI CH3
A 12	Not used	B 12	IDX HI CH3	C 13	IDX HI CH4	D 12	ENC A HI CH4	E 12	ENC A LO CH4
A 13	Not used	B 13	IDX LO CH4	C 14	ENC A LO CH5	D 13	ENC B LO CH4	E 13	ENC B HI CH4
A 14	Not used	B 14	ENC A HI CH5	C 15	ENC A HI CH6	D 14	ENC B HI CH5	E 14	ENC B LO CH5
A 15	Not used	B 15	ENC A LO CH6	C 16	ENC B LO CH6	D 15	IDX LO CH5	E 15	IDX HI CH5
A 16	Not used	B 16	ENC B HI CH6	C 17	ENC B HI CH7	D 16	IDX HI CH6	E 16	IDX LO CH6
A 17	Not used	B 17	ENC B LO CH7	C 18	IDX LO CH7	D 17	ENC A LO CH7	E 17	ENC A HI CH7
A 18	Not used	B 18	IDX HI CH7	C 19	IDX HI CH8	D 18	ENC A HI CH8	E 18	ENC A LO CH8
A 19	Not used	B 19	IDX LO CH8			D 19	ENC B LO CH8	E 19	ENC B HI CH8

Note: Do not connect to any unspecified pins

Code Table

Code	Frequency (Hz)	Notes
01	400	
02	2.8K – 3.2K	
03	2K	
04	2.69K	
05	2.5kHz	
06	7kHz	

See code list addendum for descriptions of code 50 and above

PART NUMBER DESIGNATION

64LD2- XX X X X X - XX

TOTAL NUMBER OF CHANNELS
04 = 4 Channels
08 = 8 Channels
12 = 12 Channels
16 = 16 Channels

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

MECHANICAL
F = Front Panel I/O and P2 I/O
P = P2 I/O only
W = P With Wedgelocks
A = VME64 with Blank Front Panel and P2 I/O only
B = VME64 Front Panel unshielded*** with Front Panel I/O & P2 I/O
D = VME64 with Blank Front Panel, Low profile extractors and P2 I/O only

CODE (See Code Table)

ENCODER/COMMUTATION
- = Without Encoder/Commutation option
E = With Encoder/Commutation option (Adds P0 Connector)

OPTIONAL REFERENCE SELECTION
0 = No "On Board Reference"
A = 2-28 VRMS output
C = 115 VRMS fixed output

EXCITATION CONNECTIONS
1 = One Common Excitation input tied to the Excitation Supply
2 = Individual Excitation Inputs

NOTE:
***** Unshielded to accommodate for mating 78 pin connector.**

Revision Page

Revision	Description of Change	Engineer	Date
1	Original document	FH/BC	11/14/00
1.1	Added Memory Map Title. Edited P/N, Excitation Connector Field. Corrected paging. See code list addendum for descriptions of code 50 and above. Header is 16 ch. Part Number: contact factory for other temperature requirements	GS	02/06/02
1.2	Adds Velocity & Vel. Scale registers, (A&B) res. Desc., and Encoder Option to PN.	GS	05/01/02
1.3	Removed Part Number “L” Option, VME64 front panel with Low profile extractors and with front panel I/O & P2 I/O. Front panel I/O interferes with extractors.	GS	6/19/2002
1.4	Removed 2-13.5 volt reference option (from spec, and PN)	GS	6/28/02
1.5	Standardized PN, Mech Options List to FPWABD. Mechanical Option B is unshielded to accommodate 78 pin mating connector.	GS	7/30/02
1.6	Corrected LDVT -> LVDT title for block diagrams	GS	9/18/2
1.7	Added Encoder highlights in Description section.	GS	1/7/3
1.8	Added 78 Pin connector info.	GS	5/15/3
1.9	Order option E adds P0 connector	GS	3/24/4
2.0	FOR COMMERCIAL AND MILITARY APPLICATIONS	GS	4/6/4
2.1	Added details to Interrupt Vector 1 description. Corrected Magniitude (A+B) Ch.9-16 register addresses in Memory Map.	GS	7/7/4
2.2	Max Velocity is 152.5878 SPS	GS	3/17/5
2.3	New Address	KL	04/24/07