Sixteen (16) Synchro/Resolver-to-Digital

Two-Speed or Single-Speed or Combination (Programmable)
On-Board Programmable Reference Supply
To Commercial or Military Specifications

- 16-bit resolution (optional 24 bits combined)
- ±1 arc-minute accuracy
- Continuous background BIT testing with Reference and Signal loss detection
- **Self-calibrating. Does not require removal for calibration**
- 50 Hz to 10 kHz operation
- Tracking rate to 150 RPS
- 16, 12, 8, 4 and 2-channel versions available
- Programmable 2-speed ratios: 2 to 255
- Power-On Self-Test (POST)
- Accurate Digital Velocity outputs
- Optional programmable encoder (A & B) plus index outputs
- Optional equivalent Hall Effect (A, B, C) commutation outputs
- Optional on-board programmable reference supply
- Watchdog timer and soft reset
- Angle change alert
- Transformer isolated
- Synthetic reference compensates for ±60° phase shift
- Optional conduction cooling with wedgelocks
- I/O via front panel, P2 or both
- Latch feature
- No adjustments or trimming required
- Part Number, S/N, Date Code, & Revision in non-volatile memory

DESCRIPTION:

This high density intelligent DSP-based card incorporates up to sixteen (16) single-speed or eight (8) two-speed transformer isolated Synchro/Resolver-to-Digital tracking converters with extensive diagnostics, digital velocity outputs, angle change alert, and optional programmable reference supply. Any combination of two-speed and single-speed channels can be field programmed to any ratio between 2 and 255. Each channel also produces differential (A & B) incremental encoder outputs (with programmable resolution) and a zero degree marker pulse. Alternatively, commutation outputs are available for 4, 6, or 8 pole brushless DC motors that eliminate the need for Hall Effect sensors on the motor, thus eliminating processor time and reducing bus traffic. For 2-speed usage, ambiguity circuits maintain monotonic outputs by compensating for misalignment between the Coarse and Fine Synchros. However, the processor will set a flag when it senses that the maximum allowable misalignment of 90°/gear ratio is exceeded.

This card, even when large accelerations are encountered, never looses tracking, because it incorporates the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. The LATCH feature permits the user to read all channels at the same time. Reading will unlatch that channel. The angle alert monitors each channel for the programmed angle difference and sets an interrupt as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available without interrupts or waiting time. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks. Each channel can be specified for a different voltage or frequency. A watchdog timer is provided to monitor the processor. Part number, S/N, Date Code and Revision are located in non-volatile memory.

Conduction cooling which utilizes a thermal plane and wedge locks, can be specified by adding "W" to P/N. A stiffener improves vibration response. Both sides of the board can be conformal coated (See P/N). All “E” boards are cycled from -40°C to +85°C for 24 hours.

This board incorporates major diagnostics that offer substantial improvements to system reliability, because the user is alerted to channel malfunction. This approach reduces bus traffic, because the Status Registers need not be constantly polled. Three different tests, one on-line and two off-line, can be selected:

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The (D0) Test is used to check the card and the VME interface. All channels are disconnected from the outside world, allowing the user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

Power-On Self-Test (POST): When enabled and saved, POST will initiate the D3 Test upon power-on.

SPECIFICATIONS:

Resolution:	16 bits (up to 24 bits optional for two-speed configuration)
Accuracy:	±1 arc-minute for single speed inputs ±1 arc-minute divided by the gear ratio for two-speed inputs
VME Data transfer:	Data transfers within 200 ns.
Tracking Rate:	18.5 RPS for 60 Hz version; 150 RPS for 360 Hz or greater versions. (Referred to the Fine input for two-speed configuration)
Bandwidth:	10 Hz for 60 Hz versions; 40 Hz for 400 Hz versions, & 100 Hz for greater than 1 kHz version. (also can be factory customized)
Input format:	Synchro or Resolver, (see part number)
Gear ratio:	Each channel pair is programmable from 2 to 255
Input voltage:	Resolver: 2-28 V_{L-L} Autoranging, or 90 V_{L-L} ; Synchro: 11.8 V_{L-L} , or 90 V_{L-L} Resolver and Synchro are Transformer isolated
Input Impedance:	40 kΩ min. up to 28 V_{L-L} , 100 kΩ min. at 90 V_{L-L}
Reference:	2-28 Vrms, Autoranging or 115 Vrms. Transformer isolated.
Reference Zin	100 kΩ min.
Frequency:	47 Hz to 10 kHz (see part number)
Encoder outputs:	Either 10,11,12,13,14,15 or 16-bit resolution, (field programmable) and Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N).
Commutation outputs:	Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: “Ch. Disabled”. MSB=180°; Min. differential is 0.05°. Max differential that can be programmed is 179.9°.
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Interrupts:	One Interrupt capability is implemented. One of seven priority lines can be specified.
Power:	+ 5 VDC: 0.350 A for 16 channels; ±12 VDC: 0.08 A without Reference; .600 A with 5 VA out.
Temperature, operating:	"C" 0°C to +70°C; "E" -40°C to +85°C (see part number)
Storage temperature:	-55°C to +105°C.
Conformal coating:	Both sides of the board can be conformal coated (see part number).
Temperature Cycled:	All “E” boards are cycled from -40°C to +85°C for 24 hours.
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	22 oz.

REFERENCE:	Optional. (see part number).
Voltage:	2.0-28 Vrms programmable (resolution 0.1 Vrms) or 115 Vrms fixed. Accuracy ±2%.
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5 VA max. at 40° min. inductive.

PROGRAMMING INSTRUCTIONS:

This card offers many options. Any option that is not required may be ignored. For ease of use, all channels are referred to as 1 to 16. For two-speed applications, we generally refer to Coarse and Fine inputs. Therefore, channel 1 becomes 1 Coarse, channel 2 becomes 1 Fine, channel 3 becomes 2 Coarse, etc.

I/O CONFIGURATION:

The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries (Standard), or 512 byte boundaries, when offset addresses above 100 are enabled.

A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 256 byte boundaries (Standard), or 512 byte boundaries, when offset addresses above 100 are enabled

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 256 byte boundaries (Standard), or 512 byte boundaries, when offset addresses above 100 are enabled.

Note: Address switch A8 must be set to "ON" (logic 0*)* for 512 byte boundaries.

MEMORY MAP

00	Ch.1 Data	read	44	Rev level	read	88	Angle Δ Ch.11	r/w	CC	(A&B) or A,B,C, Ch.11	r/w
02	Ch.2 Data Hi	read	46	Status, Test,	read	8A	Angle Δ Ch.12	r/w	CE	(A&B) or A,B,C, Ch.12	r/w
04	Ch.3 Data	read	48	Active channels,	r/w	8C	Angle Δ Ch.13	r/w	D0	(A&B) or A,B,C, Ch.13	r/w
06	Ch.4 Data Hi	read	4A	Save	r/w	8E	Angle Δ Ch.14	r/w	D2	(A&B) or A,B,C, Ch.14	r/w
08	Ch.5 Data	read	4C	Test (D2) verify	r/w	90	Angle Δ Ch.15	r/w	D4	(A&B) or A,B,C, Ch.15	r/w
0A	Ch.6 Data Hi	read	4E	Interrupt priority	r/w	92	Angle Δ Ch.16	r/w	D6	(A&B) or A,B,C, Ch.16	r/w
0C	Test Enable	r/w	50	Interrupt vector 1	r/w	94	Angle Δ initiate	r/w	D8	Velocity, scale Ch.1	r/w
0E	Status, Sig.	read	52	Interrupt vector 2	r/w	96	Angle change alert	read	DA	Velocity, scale Ch.2	r/w
10	Ch.7 Data	read	54	Ratio Ch 2/ Ch 1	r/w	98	(A & B) res. Ch.1	r/w	DC	Velocity, scale Ch.3	r/w
12	Ch.8 Data Hi	read	56	Ratio Ch 4/ Ch 3	r/w	9A	(A & B) res. Ch.2	r/w	DE	Velocity, scale Ch.4	r/w
14	Latch	write	58	Ratio Ch 6/ Ch 5	r/w	9C	(A & B) res. Ch.3	r/w	E0	Velocity, scale Ch.5	r/w
16	Ch.9 Data	read	5A	Ratio Ch 8/ Ch 7	r/w	9E	(A & B) res. Ch.4	r/w	E2	Velocity, scale Ch.6	r/w
18	Ch.10 Data Hi	read	5C	Ratio Ch 10/ Ch 9	r/w	A0	(A & B) res. Ch.5	r/w	E4	Velocity, scale Ch.7	r/w
1A	Status, Ref	read	5E	Ratio Ch 12/ Ch 11	r/w	A2	(A & B) res. Ch.6	r/w	E6	Velocity, scale Ch.8	r/w
1C	Velocity Ch.1	read	60	Ratio Ch 14/ Ch 13	r/w	A4	(A & B) res. Ch.7	r/w	E8	Velocity, scale Ch.9	r/w
1E	Velocity Ch.2	read	62	Ratio Ch 16/ Ch 15	r/w	A6	(A & B) res. Ch.8	r/w	EA	Velocity, scale Ch.10	r/w
20	Velocity Ch.3	read	64	Ch.13 Data	read	A8	(A & B) res. Ch.9	r/w	EC	Velocity, scale Ch.11	r/w
22	Velocity Ch.4	read	66	Ch.14 Data Hi	read	AA	(A & B) res. Ch.10	r/w	EE	Velocity, scale Ch.12	r/w
24	Velocity Ch.5	read	68	Ch.15 Data	read	AC	(A & B) res. Ch.11	r/w	F0	Velocity, scale Ch.13	r/w
26	Velocity Ch.6	read	6A	Ch.16 Data Hi	read	AE	(A & B) res. Ch.12	r/w	F2	Velocity, scale Ch.14	r/w
28	Velocity Ch.7	read	6C	Velocity Ch.13	read	B0	(A & B) res. Ch.13	r/w	F4	Velocity, scale Ch.15	r/w
2A	Velocity Ch.8	read	6E	Velocity Ch.14	read	B2	(A & B) res. Ch.14	r/w	F6	Velocity, scale Ch.16	r/w
2C	Velocity Ch.9	read	70	Velocity Ch.15	read	B4	(A & B) res. Ch.15	r/w	F8	(POST) test enable	r/w
2E	Velocity Ch.10	read	72	Velocity Ch.16	read	B6	(A & B) res. Ch.16	r/w	FA	Two speed lock loss	read
30	Velocity Ch.11	read	74	Angle Δ Ch.1	r/w	B8	(A&B) or A,B,C, Ch.1	r/w	FC	Watchdog timer	r/w
32	Velocity Ch.12	read	76	Angle Δ Ch.2	r/w	BA	(A&B) or A,B,C, Ch.2	r/w	FE	Soft reset	write
34	Test ∠	write	78	Angle Δ Ch.3	r/w	BC	(A&B) or A,B,C, Ch.3	r/w	102	Ch.2 Data Lo *	read
36	Ch.11 Data	read	7A	Angle Δ Ch.4	r/w	BE	(A&B) or A,B,C, Ch.4	r/w	104	Ch.4 Data Lo *	read
38	Ch.12 Data Hi	read	7C	Angle Δ Ch.5	r/w	C0	(A&B) or A,B,C, Ch.5	r/w	106	Ch.6 Data Lo *	read
3A	Freq.	r/w	7E	Angle Δ Ch.6	r/w	C2	(A&B) or A,B,C, Ch.6	r/w	108	Ch.8 Data Lo *	read
3C	Eo	r/w	80	Angle Δ Ch.7	r/w	C4	(A&B) or A,B,C, Ch.7	r/w	10A	Ch.10 Data Lo *	read
3E	Part #	read	82	Angle Δ Ch.8	r/w	C6	(A&B) or A,B,C, Ch.8	r/w	10C	Ch.12 Data Lo *	read
40	Serial #	read	84	Angle Δ Ch.9	r/w	C8	(A&B) or A,B,C, Ch.9	r/w	10E	Ch.14 Data Lo *	read
42	Date code	read	86	Angle Δ Ch.10	r/w	CA	(A&B) or A,B,C, Ch.10	r/w	110	Ch.16 Data Lo *	read

* Optional registers for 2-speed, extended resolution. (see Part Number)

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data° (Hi) [1]	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data° (Lo) [1]	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D1
Status, Test	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Status, Reference	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Status, Signal	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Angle change alert	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Active channels	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	Ch.13	Ch.14	Ch.15	Ch.16
Two-speed lock	X	Ch1/2	X	Ch3/4	X	Ch5/6	X	Ch7/8	X	9/10	X	11/12	X	13/14	X	15/16
(A & B) resolution [2]	X	X	X	X	X	X	X	X	X	X	X	X	X	**D2**	**D1**	**D0**

4	**16 bit**	0	0	0
6	**15 bit**	0	0	1
8	**14 bit**	0	1	0
Commutation outputs ↑	**13 bit**	0	1	1
	12 bit	1	0	0
	11 bit	1	0	1
	10 bit	1	1	0
	Encoder outputs ↑			

Notes

1 Values are rounded off and Data° (Lo) -24 bit resolution must be ordered as factory special. Consult factory for correct ordering information

2 Boards shipped after January 2004 (serial number > 17800) adds 10 and 11 bit encoder output. programmability

At **Power-ON** or **System Reset**, all parameters are restored to last saved setup and, if POST is enabled, a D3 Test is initiated.

Enter Active Channels: Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel Register*. "1"=active; "0"=not used. Omitting this step will produce false alarms, because unused channels will set faults.

Save Setup: The current setup can be saved by writing 5555h to the *Save Register*. This location will automatically clear to 0000h when the save is completed (within 5 seconds). When save is elected, all parameters are saved. However, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up.

To restore factory shipped parameters, write AAAAh to the *Save Register*, followed by System Reset. Note: After a SAVE or RESTORE, poll 4Ah and do not perform any other operation until word is at "0".

Ratio: Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Read: For single speed applications (Ratio=1), read individual channels 1,2,3,4,etc. For two-speed applications, read only channels (2,4,6,8,etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word. When data high word is read, the channel pair registers are "unlatched"

In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4,… CH15 & 16.

Two-Speed Lock-Loss: When two Synchros are geared to each other, either electrically or mechanically, in order to achieve higher accuracy, the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur, with a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss Register* will be set to "0".

Latch: Writing the integer 2 to the *Latch Register* will cause all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

Velocity Output: Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then
Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

Velocity Scale Factor: The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec resolution (lowest setting)

Power-On Self-Test (POST): Will initiate the D3 Test upon power-on, if POST is enabled and saved. Enable by writing "1" to *POST Register*. Disable by writing "0" and then save setup.

D2 Test Enable: Writing "1" to D2 of *Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. An Interrupt (if enabled) will be set to indicate an accuracy problem and the results are available in *Test Status Register* (within 45 sec). A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. Card will (every 30 seconds) write 55h to Test (D2) Verify register when D2 is enabled. User can periodically clear to Test (D2) Verify register to 0000h and then read again, after 30 seconds, to verify that background BIT testing is activated.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Reference Status Registers*.

D3 Test Enable: Writing “1” to D3 of *Test Enable Register*, initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. Test cycle is completed within 45 seconds and results can be read from the *Test Status Registers*. D3 changes from “1” to “0” when test is complete. A failure will trigger an Interrupt (if enabled). The testing requires no external programming, and can be initiated by writing "1" to D3 or terminated by writing "0" to D3.

Signal and Reference monitoring is disabled during D3 test.

D0 Test Enable: Checks card and VME interface. Writing “1” to D0 of *Test Enable Register* disconnects all channels from the outside world, enabling user to write any number of angles to the card at 34h. Data is then read from the VME interface (after writing, allow 400 ms before reading). Test accuracy to be <.05°. Disable by setting D0 to “0”. Upon writing “1”, the default test angle of D0 is 30°. External reference is <u>not</u> required. (ex. 330°=1110101010101011).

Signal and Reference monitoring is disabled during D0 test.

Status, Test: Check the corresponding bit of the *Test Status Register*, for status of BIT testing for each active channel. A ”1” means accuracy passes; A “0” indicates a failure on an active channel. Channels that are inactive are also set to “0” (test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register

Status, Ref: Check the corresponding bit of the *Ref Status Register*, for status of the reference input for each active channel. A ”1” means Reference ON, a “0” means Reference Loss on active channels. Channels that are inactive are also set to “0” (Reference loss is detected after 2 seconds). Reference monitoring is disabled during D3 or D0 Test. Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

Status, Sig: Check the corresponding bit of the *Sig Status Register*, for status of the input signals for each active channel. A "1" means Signal is valid (level must be a minimum of 2V), a “0” means Signal loss on active channels. (Signal loss is detected after 2 seconds). Channels that are inactive are also set to “0”. Signal monitoring is disabled during D3 and D0 test. Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

Interrupt Priority: Enter requirements as a 16-bit integer. 0 = no interrupt; 1-7 indicates priority levels.
Any error will latch Status Register and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, let us consider what happens when a status bit changes <u>before</u> registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms registers will be updated with the background data. Allow 250 ms to scan all channels.

Interrupt Vector 1: Write 16-bit integer (0-255). Used for failure reports.

Interrupt Vector 2: Write 16-bit integer (0-255). Used for angle change alert reports.

Angle Change Alert: Write a 16-bit word to each channel, to represent the minimum differential required. MSB=180°; minimum differential is 0.05°. Setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring by writing “1” to Angle Change Initiate Register. When that differential is exceeded, on any monitored channel, an interrupt is generated. Read Angle Change Alert Flag Register at 96h for status of each channel ("0" = no change, "1" = change)

Soft Reset: (Level sensitive): Writing a “1” initiates and holds software in reset state. Then, writing “0” initiates reboot (takes 400 ms). Status Registers cleared; Watchdog Timer functional; Failure bit at "0"; Saved parameters remain saved; Angle outputs held at last update; Interrupts disabled.

Watchdog Timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec, should look for the inverted code to confirm that the processor is operating.

Optional Reference Supply: For frequency, write a 16-bit word (Ex: 400 Hz = 1 1001 0000) to address 3A. For voltage, write a word (Ex: 26.1 Vrms =1 0000 0101) with LSB=0.1 Vrms, to address 3C. It is recommended that user program the required frequency before setting the output voltage.

Optional (A&B) Encoder Resolution: Enter required resolution, for each channel, per above table. Can be changed on the fly. Also set corresponding [(A&B) or A, B, C] register to “0”. Encoder/Commutation outputs are optional, see part ordering information. Default is 12-bit encoder mode.

Optional Commutation Outputs (A,B,C): Set channels that should produce commutation outputs to "1" in the appropriate [(A&B) or A, B, C] register. Then, set the required motor poles (per above table) in the equivalent (A&B) resolution registers. Encoder/Commutation outputs are optional, see part ordering information.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: is read as a 16-bit binary word.

Date Code: Read as a decimal number. The four digits represent YYWW (Year,Year,Week.Week)

Rev: At 44h.
Example

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1

DSP Rev 1.1 FPGA Rev 3 PC Rev 1

Front panel Connectors:

J1: DC37P; Mate: DC37S (not supplied)

37	S1	Ch. 1	15	S4	Ch. 2	28	S1	Ch. 4	6	S4	Ch. 5	37	S1	Ch. 7	15	S4	Ch. 8	28	S1	Ch.10	6	S4	Ch.11
36	S3	Ch. 1	32	RHi	Ch. 2	27	S3	Ch. 4	23	RHi	Ch. 5	36	S3	Ch. 7	32	RHi	Ch. 8	27	S3	Ch.10	23	RHi	Ch.11
19	S2	Ch. 1	14	RLo	Ch. 2	10	S2	Ch. 4	5	RLo	Ch. 5	19	S2	Ch. 7	14	RLo	Ch. 8	10	S2	Ch.10	5	RLo	Ch.11
18	S4	Ch. 1	31	S1	Ch. 3	9	S4	Ch. 4	22	S1	Ch. 6	18	S4	Ch. 7	31	S1	Ch. 9	9	S4	Ch.10	22	S1	Ch.12
35	RHi	Ch. 1	30	S3	Ch. 3	26	RHi	Ch. 4	21	S3	Ch. 6	35	RHi	Ch. 7	30	S3	Ch. 9	26	RHi	Ch.10	21	S3	Ch.12
17	RLo	Ch. 1	13	S2	Ch. 3	8	RLo	Ch. 4	4	S2	Ch. 6	17	RLo	Ch. 7	13	S2	Ch. 9	8	RLo	Ch.10	4	S2	Ch.12
34	S1	Ch. 2	12	S4	Ch. 3	25	S1	Ch. 5	3	S4	Ch. 6	34	S1	Ch. 8	12	S4	Ch. 9	25	S1	Ch.11	3	S4	Ch.12
33	S3	Ch. 2	29	RHi	Ch. 3	24	S3	Ch. 5	20	RHi	Ch. 6	33	S3	Ch. 8	29	RHi	Ch. 9	24	S3	Ch.11	20	RHi	Ch.12
16	S2	Ch. 2	11	RLo	Ch. 3	7	S2	Ch. 5	2	RLo	Ch. 6	16	S2	Ch. 8	11	RLo	Ch. 9	7	S2	Ch.11	2	RLo	Ch.12
									1	Chassis											1	Chassis	

NOTE: When a "common" reference is specified in the part number, all front panel RHi (chan1-16) will be tied together and all front panel RLo (Chan 1-16) will be tied together, and then they are connected to the optional on-board reference RHi and RLo.

J2: DC37P; Mate: DC37S (not supplied)

J3: DB25P; Mate: DB25S

Pin		Pin		Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	S1 Ch.13	14	S4 Ch.13	4	S1 Ch.14	17	S4 Ch.14	7	S1 Ch.15	20	S4 Ch.15	10	S1 Ch.16	23	S4 Ch.16	13	Chassis
2	S3 Ch.13	15	RHi Ch.13	5	S3 Ch.14	18	RHi Ch.14	8	S3 Ch.15	21	RHi Ch.15	11	S3 Ch.16	24	RHi Ch.16		
3	S2 Ch.13	16	RLo Ch.13	6	S2 Ch.14	19	RLo Ch.14	9	S2 Ch.15	22	RLo Ch.15	12	S2 Ch.16	25	RLo Ch.16		

P2 Connector: Uses a 5 row 160 pin connector

Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation
18c	S1 Ch. 1	30a	RLo Ch. 3	21a	RHi Ch. 6	4c	S4 Ch. 9	11d	S2 Ch. 12	28d	S3 Ch. 15
22c	S3 Ch. 1	18a	S1 Ch. 4	23a	RLo Ch. 6	1a	RHi Ch. 9	12d	S4 Ch. 12	29d	S2 Ch. 15
20c	S2 Ch. 1	22a	S3 Ch. 4	11a	S1 Ch. 7	2a	RLo Ch. 9	13d	RHi Ch. 12	30d	S4 Ch. 15
24c	S4 Ch. 1	20a	S2 Ch. 4	15a	S3 Ch. 7	5c	S1 Ch. 10	14d	RLo Ch. 12	5z	RHi Ch. 15
29c	RHi Ch. 1	24a	S4 Ch. 4	13a	S2 Ch. 7	6c	S3 Ch. 10	15d	S1 Ch. 13	7z	RLo Ch. 15
27c	RLo Ch. 1	27a	RHi Ch. 4	17a	S4 Ch. 7	7c	S2 Ch. 10	16d	S3 Ch. 13	9z	S1 Ch. 16
10c	S1 Ch. 2	29a	RLo Ch. 4	8a	RHi Ch. 7	8c	S4 Ch. 10	17d	S2 Ch. 13	11z	S3 Ch. 16
14c	S3 Ch. 2	10a	S1 Ch. 5	9a	RLo Ch. 7	3a	RHi Ch. 10	18d	S4 Ch. 13	13z	S2 Ch. 16
12c	S2 Ch. 2	14a	S3 Ch. 5	11c	S1 Ch. 8	4a	RLo Ch. 10	19d	RHi Ch. 13	15z	S4 Ch. 16
16c	S4 Ch. 2	12a	S2 Ch. 5	15c	S3 Ch. 8	3d	S1 Ch. 11	20d	RLo Ch. 13	17z	RHi Ch. 16
30c	RHi Ch. 2	16a	S4 Ch. 5	13c	S2 Ch. 8	4d	S3 Ch. 11	21d	S1 Ch. 14	19z	RLo Ch. 16
28c	RLo Ch. 2	21c	RHi Ch. 5	17c	S4 Ch. 8	5d	S2 Ch. 11	22d	S3 Ch. 14	19a	Int. Ref. Output Hi
25c	S1 Ch. 3	23c	RLo Ch. 5	6a	RHi Ch. 8	6d	S4 Ch. 11	23d	S2 Ch. 14	19c	Int. Ref. Output Lo
32c	S3 Ch. 3	25a	S1 Ch. 6	7a	RLo Ch. 8	7d	RHi Ch. 11	24d	S4 Ch. 14		
26c	S2 Ch. 3	32a	S3 Ch. 6	1c	S1 Ch. 9	8d	RLo Ch. 11	25d	RHi Ch. 14		
31c	S4 Ch. 3	26a	S2 Ch. 6	2c	S3 Ch. 9	9d	S1 Ch. 12	26d	RLo Ch. 14		
28a	RHi Ch. 3	31a	S4 Ch. 6	3c	S2 Ch. 9	10d	S3 Ch. 12	27d	S1 Ch. 15		

S4 pins are used only with Resolvers. Do not connect to any undesignated pins.

NOTE: P2 is always active

P0 Connector: Only supplied when (A & B) outputs are specified

1e	Ch.1 A Hi	4b	Ch.3 Index Hi	7a	Ch.6 B Hi	10d	Ch.9 A Hi	13c	Ch.11 Index Hi	17e	Ch.14 B Hi
1d	Ch.1 A Lo	4a	Ch.3 Index Lo	7b	Ch.6 B Lo	10e	Ch.9 A Lo	14c	Ch.11 Index Lo	17d	Ch.14 B Lo
1a	Ch.1 B Hi	4d	Ch.4 A Hi	7c	Ch.6 Index Hi	11e	Ch.9 B Hi	14b	Ch.12 A Hi	17a	Ch.14 Index Hi
1b	Ch.1 B Lo	4e	Ch.4 A Lo	8c	Ch.6 Index Lo	11d	Ch.9 B Lo	14a	Ch.12 A Lo	17b	Ch.14 Index Lo
1c	Ch.1 Index Hi	5e	Ch.4 B Hi	8b	Ch.7 A Hi	11a	Ch.9 Index Hi	14d	Ch.12 B Hi	17c	Ch.15 A Hi
2c	Ch.1 Index Lo	5d	Ch.4 B Lo	8a	Ch.7 A Lo	11b	Ch.9 Index Lo	14e	Ch.12 B Lo	18c	Ch.15 A Lo
2b	Ch.2 A Hi	5a	Ch.4 Index Hi	8d	Ch.7 B Hi	11c	Ch.10 A Hi	15e	Ch.12 Index Hi	18b	Ch.15 B Hi
2a	Ch.2 A Lo	5b	Ch.4 Index Lo	8e	Ch.7 B Lo	12c	Ch.10 A Lo	15d	Ch.12 Index Lo	18a	Ch.15 B Lo
2d	Ch.2 B Hi	5c	Ch.5 A Hi	9e	Ch.7 Index Hi	12b	Ch.10 B Hi	15a	Ch.13 A Hi	18d	Ch.15 Index Hi
2e	Ch.2 B Lo	6c	Ch 5 A Lo	9d	Ch.7 Index Lo	12a	Ch.10 B Lo	15b	Ch.13 A Lo	18e	Ch.15 Index Lo
3e	Ch.2 Index Hi	6b	Ch.5 B Hi	9a	Ch.8 A Hi	12d	Ch.10 Index Hi	15c	Ch.13 B Hi	19e	Ch.16 A Hi
3d	Ch.2 Index Lo	6a	Ch.5 B Lo	9b	Ch.8 A Lo	12e	Ch.10 Index Lo	16c	Ch.13 B Lo	19d	Ch.16 A Lo
3a	Ch.3 A Hi	6d	Ch.5 Index Hi	9c	Ch.8 B Hi	13e	Ch.11 A Hi	16b	Ch.13 Index Hi	19a	Ch.16 B Hi
3b	Ch.3 A Lo	6e	Ch.5 Index Lo	10c	Ch.8 B Lo	13d	Ch.11 A Lo	16a	Ch.13 Index Lo	19b	Ch.16 B Lo
3c	Ch.3 B Hi	7e	Ch.6 A Hi	10b	Ch.8 Index Hi	13a	Ch.11 B Hi	16d	Ch.14 A Hi	P2-1z	Ch.16 Index Hi
4c	Ch.3 B Lo	7d	Ch.6 A Lo	10a	Ch.8 Index Lo	13b	Ch.11 B Lo	16e	Ch.14 A Lo	P2-3z	Ch.16 Index Lo

NOTE: For commutation (A,B,C) outputs: A Hi becomes A, B Hi becomes B, and Index Hi becomes C.

The board contains two green LED's (D8 & D9) that are for factory use only. Both will be ON during normal operation. Miniature test connector, JP2 is used to download programming data and JP3 is a ground. Do not interface to these two connectors unless factory instructed to be used for field modification.

Resolver: 2-28 V_{L-L} Autoranging, 90 V_{L-L}
Synchro: 11.8 V_{L-L} , 90 V_{L-L}

Code Table

Code	Input (VL-L)	Ref (Vrms)	Frequency (Hz)
01	11.8	26	400
02	90	115	400
03	90	115	50/400
04	2-26	2-26	400
05	2-26	2-26	800
06	2-26	2-26	1000
07	2-26	2-26	1200
08	2-26	2-26	1600
09	2-26	2-26	2000
10	2-26	2-26	2500
11	2-26	2-26	3000
12	2-26	2-26	4000
13	2-26	2-26	5000
14	2-26	2-26	6500
15	2-26	2-26	7000
16	2-26	2-26	10000
17	2-26	115	400

See code list addendum for descriptions of code 50 and above.

IMPORTANT: Tracking rate and bandwidth can easily be customized to meet your specific requirements.

PART NUMBER DESIGNATION

64SD1- XX X X X X - XX

TOTAL NUMBER OF CHANNELS(*)
02 – 2 S/D Channels
04 – 4 S/D Channels
08 – 8 S/D Channels
12 – 12 S/D Channels
16 – 16 S/D Channels

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

FORMAT
S = Synchro
R = Resolver
M = Mixed (See Code Table)

(*) Number of 24 bit channels is dependant upon carrier frequency etc…consult factory for specifics

MECHANICAL
F = Front Panel I/O and P2 I/O
P = P2 I/O only
W = P With Wedgelocks
A = VME64 with Blank Front Panel and P2 I/O only
B = VME64 Front Panel with Front Panel I/O & P2 I/O
D = VME64 with Blank Front Panel, Low profile extractors and P2 I/O only

CODE (See Code Table)

OPTIONS

With On-Board Reference:
1 = One Common Reference Input Tied to On-Board Reference Supply
2 = Individual Reference Inputs
3 = One Common Reference Input Tied to On-Board Reference Supply; Programmable Encoder^2 (A & B) and Index/Commutation
4 = Individual Reference Inputs; Programmable Encoder^2 (A & B) and Index/Commutation

Without On-Board Reference:
5 = One Common Reference Input
6 = Individual Reference Inputs
7 = One Common Reference Input; Programmable Encoder^2 (A & B) and Index/Commutation
8 = Individual Reference Inputs; Programmable Encoder^2 (A & B) and Index/Commutation

Custom Design:
9 = Custom Design (See Separate Spec)

NOTE:
1. When a "common" reference is specified in the part number, all front panel RHi (chan1-16) will be tied together and all front panel RLo (Chan 1-16) will be tied together, and then they are connected to the optional on-board reference RHi and RLo.
2. Boards shipped after January 2004 (serial number > 17800) add 10 and 11 bit encoder output programmability.

Revision Page

Revision	Description of Change	Engineer	Date
1.9	Initial Release	GS	02/05/02
2	Adjusted column width in Register Bit Map	GS	04/09/02
2.1	Corrected FONTS and REGISTER BIT MAP (Encoder & Commutation "arrrow")	GS	04/23/02
2.2	Replaced 150 with 152.5878 rps. Affects Velocity Scale Factor and Vel Output Descriptions	GS	6/27/02
2.3	Standardized PN, Mech Options List to FPWABD	GS	7/30/02
2.4	Appended note 1 to REGISTER BIT MAP, "Values are rounded off and Data° (Lo) -24 bit resolution must be ordered as factory special. Consult factory for correct ordering information"	GS	4/8/3
2.5	Code 12-16: Removed "This code is available for card with a maximum of 12 channels"	GS	9/19/3
2.6	Boards shipped after January 2004 (serial number > 17800) add 10 and 11 bit encoder output programmability.	GS	1/8/4
2.7	FOR COMMERCIAL AND MILITARY APPLICATIONS. If enabled, D2 Test Enable will write 55h to Test (D2) Verify register approximately every 30s.	GS	3/17/5
2.8	Corrected 2-speed 24 bit read: Data Lo, when read, latched data Hi. Data Hi read "unlatches" (pg. 5).	AS	4/11/06
2.9	New Address	KL	04/24/07