Eight (8) Digital-to-Synchro/Resolver (1.2 VA)

TWO-SPEED OR SINGLE SPEED OR COMBINATION (PROGRAMMABLE)
16 BIT RESOLUTION; WRAP-AROUND SELF TEST, PROGRAMMABLE ROTATION
FOR COMMERCIAL AND MILITARY APPLICATIONS

FEATURES:

- 16-bit resolution
- 30 arc-seconds accuracy
- Continuous background BIT testing with Reference and Signal loss detection
- Power-On Self-Test (**POST**)
- Programmable 2-speed ratios (2 to 255) and angle rotation
- Outputs can be turned ON/OFF
- Redundant operation available (Contact factory)
- 360 Hz to 10 kHz operation
- Optional on-board programmable reference supply
- Transformer isolated
- Watchdog timer and soft reset
- 8, 6, 4 and 2-channel versions available
- Either A32, A24 or A16 address
- Geographical addressing
- I/O via front panel, P2, or both
- No adjustments or trimming required
- Part Number, S/N, Date Code, & Revision in non-volatile memory

DESCRIPTION:

This high density intelligent DSP-based card incorporates up to eight separate transformer isolated Digital-to-Synchro/Resolver converters with 1.2 VA drive, extensive diagnostics, signal & reference loss detection and optional 5 VA reference supply. Either one common or eight separate reference inputs can be specified. This card offers two-speed configuration and constant rotation that includes a start and a stop angle. Transformer isolation enables user to ground one of the outputs without effecting performance. External amplifiers, to handle 30 VA from 50 Hz to 400 Hz, can seamlessly be integrated. The optional on–board reference is field programmable for both voltage and frequency. If geographical addressing is part of your system, this card will respond, otherwise the board dip switches will be activated to set the base address. A watchdog timer is provided to monitor the processor. This model will drive passive loads such as CT's etc. A green LED is provided, on front panel models only, to visually indicate o.k. status (reference and signal present and no fault.) Part Number, S/N, Date Code and Revision are located in permanent memory locations.

Major diagnostics are incorporated to offer substantial improvements to system reliability because user is alerted (within 5 seconds) to channel malfunctions. This approach reduces bus traffic because the Status Registers do not require constant polling. See Programming Instructions for further details.

The D2 Test initiates automatic background BIT testing that compares the output of each channel against the commanded input to a test accuracy of 0.05° and monitors each Output and Reference. A failure triggers an Interrupt (if enabled) and results are available in Status Registers. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 Test starts a BIT Test that generates and tests 72 different angles, to a testing accuracy of 0.05°. Results can be read from Status Registers. External reference is required. Testing requires no external programming, and can be Initiated or terminated via the bus. CAUTION: Outputs are active during this test. Check connected loads for possible interaction.

Power-On Self-Test (POST), if enabled, initiates the D3 Test upon turn-on and is enabled/disabled via the bus.

Conduction cooling which utilizes a thermal plane and wedge locks, can be specified (See P/N.) A stiffener improves vibration response. Both sides of the board can be conformal coated (See P/N). All "E" boards are cycled from -40°C to +85°C for 24 hours.

SPECIFICATIONS	(applies to each channel)
Resolution:	16 bits (.0055°)
Accuracy:	30 arc-seconds (.0083°) at 0.3 VA. ±1 arc-minute (.017°) at 1.2 VA worst case.
Output format:	(See part number), transformer isolated
Output voltage:	(See code table and part number).
Output load:	1.2 VA max./Channel. Short circuit protected. (5000 Ω reactive at 90 V_{L-L} Synchro, 90 Ω reactive at 11.8 V_{L-L} Synchro, 110 Ω reactive at 11.8 V_{L-L} Resolver)
Regulation:	5% max. No load to Full load
Ratio:	Set any ratio between 2 and 255
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 rps with a resolution of 0.15°/sec. Step size is 16 bits (0.0055)° up to 1.5 rps, then linearly increases to 12 bits (0.088°) at 13.6 rps.
Reference input voltage:	(See part number), transformer isolated. Uses 1 ma max. /Channel
Reference frequency:	360 Hz to 10 kHz (See part number)
Phase shift:	5° max. between output and reference.
Settling time:	Less than 100 microseconds
Base address:	Responds to geographical addressing. Otherwise, the dipswitches are activated for setting the base address.
VME Data transfer:	Data transfers within 200 ns
Interrupts:	Interface implements a single Interrupt capability. One of seven priority lines can be selected.
Power: (From P1)	+ 5 VDC at 0.4 A ±12 VDC at 1.6 A average, 4.0 A peak (for 8 channels) Power supplies must be able to supply peak power without current limiting..
Temperature, operating:	"C" = 0°C to +70°C; "E" = -40°C to +85°C (See part number)
Temperature, storage:	-55°C to +105°C
Humidity:	95% non-condensing
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	27 oz. (8 channel)

REFERENCE:	Optional. (See part number).
Voltage:	2.0-28 Vrms programmable (resolution 0.1 Vrms) or 115 Vrms fixed. Accuracy ±2%.
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5 VA max. at 40° min. inductive.

PROGRAMMING INSTRUCTIONS:

I/O CONFIGURATION:

The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries.

A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 256 byte boundaries.

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 256 byte boundaries.

Geographical Addressing: When Geographical Addressing is enabled (see P/N), the card will respond to address modifier 2Fh for A24 Address mode, where the 5 SB's of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:

1) the base address the card should to respond to
2) the address modifier (A16, A24, A32)
3) then enable the card.

For example : If the card is in slot # 10 the 5 MSB's are 01010 so the address of the CSR registers are :
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)
Write to address 57FF63 h, the A31 – A24 base address bits, for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h the address modifier you wish to respond to shifted up 2 bits, ex. 28h(0A<< 2)
Then Write to address 57FFFBh , 10h to enable the card.
The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

MEMORY MAP

00	Ch.1	read/write	34	Wrap-around Ch. 3	read	72	Rotation, Initiate,	write
02	Ch 2	read/write	36	Wrap-around Ch. 4	read	74	Rotation, Stop	write
04	Ch.3	read/write	38	Wrap-around Ch. 5	read	76	Rotation completed [1]	read
06	Ch.4	read/write	3A	Wrap-around Ch. 6	read	80	Ratio, Ch.1/2	read/write
08	Ch.5	read/write	3C	Wrap-around Ch. 7	read	82	Ratio, Ch.3/4	read/write
0A	Ch.6	read/write	3E	Wrap-around Ch. 8	read	84	Ratio, Ch.5/6	read/write
0C	Ch.7	read/write	50	Stop angle Ch.1	read/write	86	Ratio, Ch.7/8	read/write
0E	Ch.8	read/write	52	Stop angle Ch2	read/write	88	Status, Ext. amp.	read
10	Status, Signal	read	54	Stop angle Ch.3	read/write	90	Outputs ON/OFF	read/write
12	Status, Reference	read	56	Stop angle Ch.4	read/write	92	External / Internal	read write
14	Status, Test	read	58	Stop angle Ch.5	read/write	94	Power-on POST test	read/write
16	Part number	read	5A	Stop angle Ch.6	read/write	96	Ref Supply Freq.	read/write
18	Serial number	read	5C	Stop angle Ch.7	read/write	98	Ref Supply Voltage	read/write
1A	Date code	read	5E	Stop angle Ch.8	read/write	9A	Watchdog timer	read/write
1C	Rev level	read	60	Rotation rate, Ch.1	read/write	9C	Soft reset	write
1E	Test (D2) verify	read/write	62	Rotation rate Ch.2	read/write	A0	Current Position Ch.1	read
20	Interrupt Level	read/write	64	Rotation rate Ch.3	read/write	A2	Current Position Ch.2	read
22	Interrupt Vector	read/write	66	Rotation rate Ch.4	read/write	A4	Current Position Ch.3	read
28	Active channels	read/write	68	Rotation rate Ch.5	read/write	A6	Current Position Ch.4	read
2C	Save	read/write	6A	Rotation rate Ch.6	read/wri	A8	Current Position Ch.5	read
2E	Test enable	read/write	6C	Rotation rate Ch.7	read/wri	AA	Current Position Ch.6	read
30	Wrap-around Ch. 1	read	6E	Rotation rate Ch.8	read/wri	AC	Current Position Ch.7	read
32	Wrap-around Ch. 2	read	70	Rotation, Mode	read/wri	AE	Current Position Ch.8	read

Note 1. Implemented as of October 2004

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data [2]	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Current Position [2]	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Outputs, ON/OFF	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Rotation, Mode	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Rotation, INITIATE	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Rotation, STOP	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Rotation completed	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Active channels	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Status, Reference	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Status, Signal	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Status, Test	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
External/Internal	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X
Status, Ext. amp.	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	X	X	X	X	X	X	X	X

Note 2. Approximate Values

At **Power-On** or **System Reset**, all parameters are restored to last saved setup and if POST is enabled, a D3 Test is initiated.

Enter Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel Register at 28h. “1”=active; “0”=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: The current setup can be saved by writing 5555h to initialize the Save Register. This location will automatically clear to 0000h when the save is completed (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up.
To restore factory shipped parameters, write AAAAh to the Save Register followed by System Reset. Note: After a SAVE or RESTORE, poll the Save Register and do not perform any other operation until word is at "0".

Enter Interrupt Levels as an 16-bit binary number. 0= no interrupt; 1-7 indicates priority levels.
Any error will latch Status Register and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. After reading, registers will be updated with the background data within 250ms.

Interrupt Vector: Write 16-bit word (0-255) to Interrupt Vector Register.

Write Angle – Single Speed:

For single-speed applications (Ratio=1), write a 16-bit integer (or 16-bit 2’s compliment integer) to the corresponding channel *Data Register.* (ex. 330° = EAABh).
WORD = (Angle ÷ ($360/2^{16}$)).
Note: writing to an Input Angle Register will stop any rotation initiated on that channel

Current Position

Read Current Position Register to determine the current position simulated by that DS channel. Especially useful for rotation applications. Read as16-bit integer (or 16-bit 2’s compliment integer). WORD = (Angle ÷ ($360/2^{16}$)).

Write Angle – Two-Speed:

In two-speed applications, the ratio will affect the fine speed output resolution. (Higher ratios result in lower resolutions at the output.) This occurs from multiplying the coarse angle by the ratio to achieve the fine angle output. This multiply reduces the overall resolution by increasing the weight of the LSB’s. To compensate for this, the card allows for 24-bit resolution for the higher ratios. This feature is transparent and automatic to the user and will regain the resolution needed in higher ratio systems.

When 16 bit resolution is sufficient, the angle can be represented by first writing the integer 0 to the even channel of the pair *Data Register,* then a 16-bit integer (or 16-bit 2’s compliment integer) to the odd channel of the pair (coarse speed) *Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. Note: Integer 0 only needs to be written to the even channel once to initialize the even channel register. Subsequently, only writes to the odd channel are necessary.

Odd Channel	Even Channel
16 Bits	0

16 bit integer = Angle / ($360/2^{16}$); Fine Speed ≡ Angle * Ratio / ($360/2^{16}$)

Ex1. For a ratio of 255, the fine speed output would have a resolution of 1.4008°.
Thus, for every 0.00549° of shaft angle, the fine output will change in 1.4008° increments.

When 24 bit resolution is desired, the angle can be represented as a 24-bit integer (or 24-bit 2’s compliment integer) by first writing the lower 8-bits to the upper byte of the even channel of the pair of the *D/S Data Register*, then the upper 16-bits to the odd channel of the pair (coarse speed) of the *D/S Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. The channel pairs are defined as Ch1&2, Ch3&4, Ch5&6 and Ch7&8.

Odd Channel	Even Channel	
16 Bits	8 Bits	X

24 bit integer = Angle / ($360/2^{24}$); Fine Speed ≡ Angle * Ratio / ($360/2^{24}$)
Ex1. For a ratio of 255, the fine speed output would have a resolution of 0.00547°.
Thus, for every 0.000021458° of shaft angle, the fine output will change in 0.00547° increments.

Note: Writing to an input angle register will stop any rotation initiated on that channel.

Ratio: Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

ON/OFF: Set the bit, corresponding to each channel to be turned on, to “1” in Outputs On/Off Register at 90h. To turn OFF a channel, set corresponding bit to “0”. Default is OFF.

Read Wrap-Around Angles: AVAILABLE AT ALL TIMES.

Rotation Rate: Write to the corresponding Rotation Rate Register a 2’s compliment number representing the desired rotation rate, LSB = 0.15°/sec.
Ex: 12 RPS =. (12 x 360°/0.15° = 28800 = 7080h), -12 rps = (-12 x 360°/0.15° = -28800 = 8F80h)
Step size is 16 bits (0.0055°) for up to 1.5 rps, then linearly increases to 12 bits (0.088°) at 13.6 rps.

Rotation Mode, Continuous or Start/Stop: For continuous rotation, set the corresponding channel bit to "0" in the register. For rotation to cease at a designated stop angle, set the bit to "1"

Write Stop angles: Write 16-bit binary data to appropriate address. After a channel reaches the stop angle it will stop rotating, and remain at that angle until a new input angle is set. If rotation is initiated again, the angle will start rotating from the present angle.

Initiate Rotation: First set the Rotation Rate Registers, and Rotation Mode Register, for each channel that is to rotate. Then, to start rotation for those channels, set the corresponding channel bit to a “1” in the Rotation Initiate Register.

Stop Rotation: Set the corresponding bit, for each channel to be stopped, to a “1” in the Rotation Stop Register. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated.

Rotation Completed: Read the Rotation Completed Register. Each bit corresponds to a given channel, "1" = rotation completed, "0"=rotation in process. (Implemented as of October 2004).

D2 Test Enable: Writing “1” to D2 of Test Enable Register initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the commanded angle. An Interrupt (if enabled) will be set to indicate an accuracy problem and the results can be read from Status Registers within 2 seconds. A “0” deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Outputs must be ON for test to function. Card will write 55h (every 2 seconds) to D2 Test Verify Register when D2 is enabled. User can periodically clear to 00h and then read the Test Verify Register again, after 2 seconds, to verify that BIT testing is activated. This test continuously sequences between the eight channels on the card with each output being measured for approx. 180 mSec. If the measured angle has an error greater the 0.05º (0.2º for external amplifiers), a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Reference Status Registers*.

D3 Test Enable: Writing “1” to D3 of Test Enable Register initiates a BIT test that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is required and outputs must be ON. An Interrupt (if enabled) will be set to indicate an accuracy problem or Signal or Reference loss. Results are available in Status Registers. Test cycle takes about 30 seconds and D3 changes from “1” to “0” when test is complete. The testing requires no external programming, and can be terminated at any time by writing a “0” to D3 bit of the *Test Enable Register*. CAUTION: Outputs must be ON during this test and are therefore active. Check connected loads for possible interaction.

Power-On Self-Test (POST): Will initiate the D3 Test on Power-On, if POST is enabled and saved. Enable by writing "1" or Disable by writing "0" to POST Register and then Save Setup.

Status, Test: Check the corresponding bit of the Test Status Register, for status of BIT testing for each active channel. A ”1” Accuracy OK; “0” failed. (test cycle takes 2 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register. Front Panel LED indicates status o.k. (reference and signal and test o.k.).

Status, Ref: Check the corresponding bit of the *Reference Status Register* for status of the reference input for each active channel. A ”1” means Reference ON, “0” means Reference Loss on active channels. Channels that are inactive are also set to “0”. (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register. Front Panel LED indicates status o.k. (reference and signal and test o.k.).

Status, Sig: Check the corresponding bit of the *Signal Status Register* for status of the output signals for each active channel. A "1" means Signal is valid, “0” means Signal loss. Channels that are inactive are also set to “0”. (Signal loss is detected after 2 seconds). Signal monitoring is always enabled. Any Signal status failure, transient or

intermittent will latch the *Signal Status Register*. Reading will unlatch register. Front Panel LED indicates status o.k. (reference and signal and test o.k.).

Status, Ext. Amp: Check the corresponding bit of the Ext Amp Status Register, for status of BIT testing for each active channel that has the External Amp enabled. A ”1” Accuracy OK; “0” failed. Any Ext Amp status failure, transient or intermittent will latch the *Ext Amp Status Register*. Reading will unlatch register.

External/Internal: When wrap-around BIT test capability is required for external Synchro amplifiers, set the bit, corresponding to each channel that has an external amplifier to be monitored, to “1” in the External/Internal register. Default is Internal.

Soft Reset (Level sensitive): Writing “1” initiates and holds software reset state. Then, writing “0” initiates reboot (takes 400 ms). Power-On or a hardware RESET, sets ’reset’ bit to “0”. Following the soft reset, a power on automatic calibration test is run and completes in approximately 10 seconds. This function is equivalent to Power on Reset.

Watchdog Timer: This feature monitors the watchdog timer register. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec. should look for the inverted code to confirm that the processor is operating.

Optional Reference Supply: For frequency, write a 16-bit word (Ex: 400 Hz = 1 1001 0000.
For voltage, write an 16-bit word (Ex: 26.1 Vrms =1 0000 0101) with LSB=0.1 Vrms. It is recommended that user program the required frequency before setting the output voltage. Output at P2-1d & 2d and/or J1-17 & 35

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: is read as a 16-bit binary word.

Date Code: Read as a decimal number. The four digits represent YYWW (Year,Year,Week.Week)

Revision Level:
Example

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1

DSP Rev 1.1 FPGA Rev 3 PC Rev 1

Panel Connectors:

J1: DC37P; Mate: DC37S

Pin	Ch.1	Pin	Ch.2	Pin	Ch.3	Pin	Ch.4	Pin	Ch.5	Pin	Ch.6
37	S1	34	S1	31	S1	28	S1	24	S1	21	S1
36	S2	33	S2	30	S2	27	S2	25	S2	22	S2
19	S3	16	S3	13	S3	10	S3	7	S3	4	S3
18	S4	15	S4	12	S4	9	S4	6	S4	3	S4
35	RHi	32	∗RHi	29	∗RHi	26	∗RHi	5	∗RHi	2	∗RHi
17	RLo	14	∗RLo	11	∗RLo	8	∗RLo	23	∗RLo	20	∗RLo
1	Chassis										

J2: DC37P; Mate: DC37S

Pin	Ch.7	Pin	Ch.8	Pin	Ext. amp	Pin	Ext. amp	Pin	Ext. amp
6	S1	10	S1	1	Sine Hi Ch.1	23	Cos Hi Ch.3	17	Common
8	S2	12	S2	2	Common	13	Sine Hi Ch.4	35	Cos Hi Ch.6
7	S3	11	S3	20	Cos Hi Ch.1	14	Common	18	Sine Hi Ch.7
27	S4	31	S4	3	Sine Hi Ch.2	32	Cos Hi Ch.4	19	Common
25	∗RHi	29	∗RHi	21	Common	15	Sine Hi Ch.5	36	Cos Hi Ch.7
26	∗RLo	30	∗RLo	22	Cos Hi Ch.2	33	Common	24	Sine Hi Ch.8
37	Chassis			4	Sine Hi Ch.3	34	Cos Hi Ch.5	9	Common
				5	Common	16	Sine Hi Ch.6	28	Cos Hi Ch.8

P2 Connector: 160 pin

Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation
18c	S1 Ch. 1	12a	S2 Ch. 5	1c	S1 Ch. 6	9d	Sine Hi Ch.3	1z	On/Off Hi Ch.1	1a	BIT Hi Ch. 1
22c	S3 Ch. 1	16a	S4 Ch. 5	2c	S3 Ch. 6	10d	Common	3z	On/Off Lo Ch.1	2a	BIT Lo Ch. 1
20c	S2 Ch. 1	29c	RHi Ch. 1	3c	S2 Ch. 6	11d	Cos Hi Ch.3	5z	On/Off Hi Ch.2	3a	BIT Hi Ch. 2
24c	S4 Ch. 1	27c	RLo Ch. 1	4c	S4 Ch. 6	12d	Sine Hi Ch.4	7z	On/Off Lo Ch.2	4a	BIT Lo Ch. 2
10c	S1 Ch. 2	28c	∗RHi Ch. 2	11a	S1 Ch. 7	13d	Common	9z	On/Off Hi Ch.3	5a	BIT Hi Ch. 3
14c	S3 Ch. 2	30c	∗RLo Ch. 2	15a	S3 Ch. 7	14d	Cos Hi Ch.4	11z	On/Off Lo Ch.3	5c	BIT Lo Ch. 3
12c	S2 Ch. 2	31a	∗RHi Ch. 3	13a	S2 Ch. 7	15d	Sine Hi Ch.5	13z	On/Off Hi Ch.4	6a	BIT Hi Ch. 4
16c	S4 Ch. 2	32a	∗RLo Ch. 3	17a	S4 Ch. 7	16d	Common	15z	On/Off Lo Ch.4	6c	BIT Lo Ch. 4
25c	S1 Ch. 3	30a	∗RHi Ch. 4	11c	S1 Ch. 8	17d	Cos Hi Ch.5	17z	On/Off Hi Ch.5	7a	BIT Hi Ch. 5
32c	S3 Ch. 3	29a	∗RLo Ch. 4	15c	S3 Ch. 8	18d	Sine Hi Ch.6	19z	On/Off Lo Ch.5	7c	BIT Lo Ch. 5
26c	S2 Ch. 3	28a	∗RHi Ch. 5	13c	S2 Ch. 8	19d	Common	21z	On/Off Hi Ch.6	8a	BIT Hi Ch. 6
31c	S4 Ch. 3	27a	∗RLo Ch. 5	17c	S4 Ch. 8	20d	Cos Hi Ch.6	23z	On/Off Lo Ch.6	8c	BIT Lo Ch. 6
18a	S1 Ch. 4	25a	∗RHi Ch. 6	3d	Sine Hi Ch.1	21d	Sine Hi Ch.7	25z	On/Off Hi Ch.7	9a	BIT Hi Ch. 7
22a	S3 Ch. 4	26a	∗RLo Ch. 6	4d	Common	22d	Common	27z	On/Off Lo Ch.7	9c	BIT Lo Ch. 7
20a	S2 Ch. 4	19a	∗RHi Ch. 7	5d	Cos Hi Ch.1	23d	Cos Hi Ch.7	29z	On/Off Hi Ch.8	21a	BIT Hi Ch. 8
24a	S4 Ch. 4	23a	∗RLo Ch. 7	6d	Sine Hi Ch.2	24d	Sine Hi Ch.8	31z	On/Off Lo Ch.8	23c	BIT Lo Ch. 8
10a	S1 Ch. 5	19c	∗RHi Ch. 8	7d	Common	25d	Common	1d	Internal Ref. Out HI		
14a	S3 Ch. 5	21c	∗RLo Ch. 8	8d	Cos Hi Ch.2	26d	Cos Hi Ch.8	2d	Internal Ref. Out Lo		

S4 pins used only with Resolvers. BIT inputs are used for external amplifiers. Do not connect to any undesignated pins.

NOTE: P2 is ALWAYS active

For Code 72 and 73 implementations (as well as old PN VME-DSFC29),
S3 = - sin S1= + sin S2 = - cos S4 = + cos

* These inputs are supplied only as individual reference inputs when specified in the part number. When references are specified as 'common' they are connected to pins 17&35 or 29c&27c respectively. If the internal reference generator is ordered, that reference voltage will **go out** on pins 1d/2d. If specified in P/N, the internal Reference can also be connected internally to all channels. If individual references are selected, then each can be connected to a different source.

The board contains two green LED's that are for factory use only. Two miniature test connectors, are used to download programming data. Do not interface to these two connectors unless factory instructed to be used for field modification.

Code Table

Code	Output (VL-L)	Ref (Vrms)	Frequency (Hz)	Load (VA)	Notes
01	11.8	26	400	1.2	
02	90	115	400	1.2	
25	2.0	2.0	7200	1.2	
26	2.0	6.0	4000	1.2	
27	2.0	8.0	2400	1.2	
28	2.0	11.8	2400	1.2	
29	3.5	7.07	3000	1.2	
31	6.8	115	400	1.2	
32	10.0	10.0	400	1.2	
33	11.8	11.8	2500	1.2	
34	11.8	115	400	1.2	

See code list addendum for descriptions of code 50 and above
Contact factory for other combinations.

PART NUMBER DESIGNATION

64DS1- X X X X X X - XX

TOTAL NUMBER OF CHANNELS
2 = 2 D/S Channels
4 = 4 D/S Channels
6 = 6 D/S Channels
8 = 8 D/S Channels

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

FORMAT
S = Synchro
R = Resolver
M = Mixed (Defined in Code Table)
1 = S With Geographical Addressing
2 = R With Geographical Addressing
3 = M With Geographical Addressing

MECHANICAL
F = Front Panel I/O and P2 I/O
P = P2 I/O only
W = P With Wedgelocks
A = VME64 with Blank Front Panel and P2 I/O only
B = VME64 Front Panel with Front Panel I/O & P2 I/O
D = VME64 with Blank Front Panel, Low profile extractors and P2 I/O only

CODE (See Code Table)

OPTIONS 2
0 = None
1 = With Output Transformer Disconnect and Redundant Capability (consult factory for operation)
9 = Custom Design (See Separate Spec)

OPTIONS 1

With On-Board Reference:
1 = One Common Reference tied to the On-Board Reference Supply
2 = Individual Reference Inputs
5 = On-Board Reference connected to 1d/2d only. All input references are tied together but not to the On-Board Reference.

Without On-Board Reference:
3 = One Common Reference Input
4 = Individual Reference Inputs

Revision Page

	Description of Change	Engineer	Date
1.4	Added Code 61	GS	12/13/01
1.5	Changed dotted to solid lines in charts for smaller/faster pdf generation	GS	01/08/02
1.6	See code list addendum for descriptions of code 50 and above. Replaced references to temperature M with temperature E. Removed J = M With Permanent Conformal Coating.	GS	02/05/02
1.7	Following the soft reset, a cal is run and completes in approximately 10 seconds.	GS	03/21/02
1.8	Added P to P2 Connected Title. Correct PN, Mech, V. …and P2 I/O	GS	6/27/02
1.9	Standardized PN, Mech Options List to FPWABD	GS	7/30/02
2.0	A green LED is provided, on front panel models only, to visually indicate power applied to the card	GS	10/24/02
2.1	PN Opt 5 = On-Board Reference connected to 1d/2d only. All input references are tied together but not to the On-Board Reference.	GS	7/1/3
2.2	For Code 72 and 73 implementations (as well as old PN VME-DSFC29); S3 = - sin, S1= + sin, S2 = - cos, S4 = + cos . A green LED is provided, on front panel models only, to visually indicate o.k. status (reference and signal present and no fault.)	GS	11/5/3
2.3	FOR COMMERCIAL AND MILITARY APPLICATIONS	GS	4/6/4
2.4	Adds Current Position Register and Rotation complete for cards newer than 10/04	GS	10/6/4
2.5	Added unit weight (8 ch configuration) (pg. 2 – Specifications)	ARS	19 Oct 05
2.6	New Address	KL	04/24/07