Model VME-64DL1

Eight (8) 3 or 4-Wire or Sixteen 2-Wire (16) Programmable
Digital-to-LVDT/RVDT Channels

LVDT Stimulus Channels

Eight (8) 3 or 4-Wire or Sixteen (16) 2-Wire, Programmable

16 BIT RESOLUTION; WRAP-AROUND SELF TEST

Optional Excitation Supply

FOR COMMERCIAL AND MILITARY APPLICATIONS

FEATURES:

- 16-bit resolution
- Continuous background BIT testing with Reference loss detection
- Power-On (**POST**) test
- Transformer isolated
- Stable output with temperature
- Watchdog timer and soft reset
- Either A32, A24 or A16 address
- Geographical addressing
- I/O via front panel, P2, or both
- No adjustments or trimming required
- Commercial or severe environment MIL
- Part number, S/N, Date code, & Rev. in non-volatile memory

DESCRIPTION:

This card offers sixteen (16) two-wire or eight (8) three/four-wire transformer isolated "PROGRAMMABLE" LVDT/RVDT outputs with wrap-around self test and optional excitation supply. Instead of buying cards that are set for specific outputs, the uniqueness of this design makes it possible to buy our generic card that can be programmed and reprogrammed in the field for any excitation and signal voltage between 2.0 and 28 volts. Operating frequency between 400 Hz and 10 KHz can be specified (see Part Number). One transformer isolated excitation is supplied for each A, B output pair. The output format of this card can be wired for either two-wire or three/four-wire. The transformation ratio (TR), same for each pair of outputs, sets the maximum output voltage with relation to the excitation voltage (TR = Max Output Voltage / Excitation Voltage). Use of a ratiometric design eliminates errors caused by excitation voltage variations. The outputs are stable with temperature and switching spikes are not noticeable**.** If geographical addressing is part of the overall system, this card will respond, otherwise the board dip switches will be activated to set base address. A watchdog timer is provided to monitor the processor. To simplify logistics, Part number, S/N, Date code, & Rev. are stored in non-volatile memory locations.

Major diagnostics are incorporated to offer substantial improvements to system reliability because user is alerted (within 5 seconds) to channel malfunctions. This approach reduces bus traffic because the Status registers do not require constant polling. **See Programming Instructions for further details**.

The (D2) test initiates automatic background BIT testing that compares the output of each channel against the commanded input to a test accuracy of 0.2 FS and monitors each Output and Excitation. A failure triggers an Interrupt (if enabled) and results are available in Status registers. Testing, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The (D3) test, starts a BIT test that generates and tests 20 different positions to a testing accuracy of 0.2 FS. Results can be read from Status registers. External reference is required. Testing requires no external programming, and can be Initiated or terminated via the bus. **CAUTION:** Outputs are active during this test. Check connected loads for possible interaction.

The POST test, when enabled, will initiate a D3 test at power turn on.

Conduction cooling which utilizes a thermal plane and wedge locks, can be specified (See P/N.) A stiffener improves vibration response. Both sides of the board can be conformal coated (See P/N.) All "E" boards are burned in for 24 hours and cycled from -40°C to +85°C.

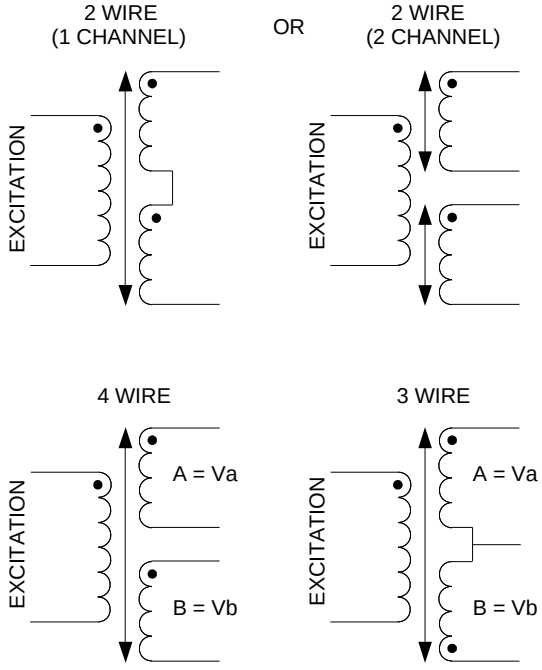
SPECIFICATIONS:

Resolution:	16 bits (.001526% FS)
Linearity:	0.1% FS for .2 <= TR <= 2.0 (.05% FS available at a specified frequency and TR)
Output Format:	Configurable for either 3/4-wire or 2-wire.Transformer isolated. Output voltage will vary directly with excitation.
Output voltage:	±24 Vrms ±1% at no load. Transformer isolated.
Load:	With output voltages from 2.0 to 20.0 Vrms: 10 kΩ min. With output voltages from 20 to 28.0 Vrms: 15 kΩ min. Short circuit protected.
Regulation:	2% max.
Excitation:	2.0 to 28 Vrms. Transformer isolated.
Frequency (excitation):	360 Hz to 10 KHz,
Phase Shift (input to output):	3° max
Phase shift (A/B):	0.5°.
Excitation (each) Z in:	50 KΩ min.
VME Data transfer:	**Data transfers within 200 ns**
Interrupts:	Interface implements a single Interrupt capability. One of seven priority lines can be selected.
Power:	+5 VDC ±5% at 0.35 A ±12 VDC ±5% at 0.5 A
Temperature, operating:	"C" 0°C to +70°C, "E" -40°C to +85°C (See part number)
Temperature, storage:	-55°C to +105°C
Size:	6U (9.2" height), 4HP (0.8") width; 233.4 mm x 20.3 mm x 160 mm deep

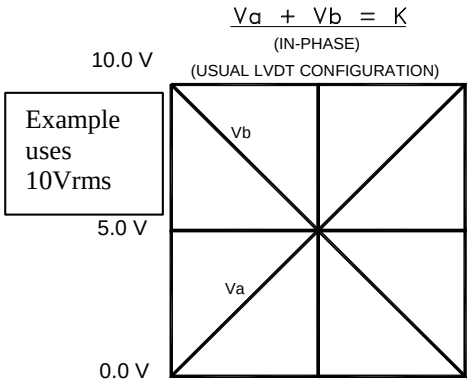
REFERENCE:

	Optional. (See part number).
Voltage:	2.0-28 Vrms programmable (resolution 0.1 Vrms). Accuracy ±2%.
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5 VA max. at 40° min. inductive.

Principal of Operation (LVDT): Typically the primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.



POSITION = (Va- Vb) / (Va+Vb)



Va+Vb=10V	Va+Vb=10V	Va+Vb=10V
Va-Vb=-10V	Va-Vb=0V	Va-Vb=10V
Va=0V	Va=5V	Va=10V
Vb=10V	Vb=5V	Vb=0V

I/O CONFIGURATION:

The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 512 byte boundaries (legacy cards DOM 0848 and earlier were 256 byte boundaries).

A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 512 byte boundaries (legacy cards DOM 0848 and earlier were 256 byte boundaries).

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 512 byte boundaries (legacy cards DOM 0848 and earlier were 256 byte boundaries).

Geographical Addressing: When Geographical Addressing is enabled (see P/N), the card will respond to address modifier 2Fh for A24 Address mode, where the 5 Msb's of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:

1) the base address the card should to respond to
2) the address modifier (A16, A24, A32)
3) then enable the card.

For example : If the card is in slot # 10 the 5 Msb's are 01010 so the address of the CSR registers are :
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)
Write to address 57FF63 h, the A31 – A24 base address bits , for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h the address modifier you wish to respond to shifted up 2 bits , for example 28h(0A<< 2)
Then Write to address 57FFFBh , 10h to enable the card.

The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

MEMORY MAP

00	Position Data Ch.1A	read/write	28	Wrap-around Ch. 3A	read	50	2-3/4 Wire Mode	read/write
02	Position Data Ch.1B	read/write	2A	Wrap-around Ch. 3B	read	52	Status, Excitation	read
04	Position Data Ch.2A	read/write	2C	Wrap-around Ch. 4A	read	54	Status, Test	read
06	Position Data Ch.2B	read/write	2E	Wrap-around Ch. 4B	read	56	Status, Signal	read
08	Position Data Ch.3A	read/write	30	Wrap-around Ch. 5A	read	58	Interrupt Level	read/write
0A	Position Data Ch.3B	read/write	32	Wrap-around Ch. 5B	read	5A	Interrupt Vector	read
0C	Position Data Ch.4A	read/write	34	Wrap-around Ch. 6A	read	5C	Active channels	read/write
0E	Position Data Ch.4B	read/write	36	Wrap-around Ch. 6B	read	5E	Test Enable	read/write
10	Position Data Ch.5A	read/write	38	Wrap-around Ch. 7A	read	60	Test (D2) verify	read/write
12	Position Data Ch.5B	read/write	3A	Wrap-around Ch. 7B	read	62	POST test	read/write
14	Position Data Ch.6A	read/write	3C	Wrap-around Ch. 8A	read	64	Freq.	read/write
16	Position Data Ch.6B	read/write	3E	Wrap-around Ch. 8B	read	66	Eo	read/write
18	Position Data Ch.7A	read/write	40	TR Ch.1	read/write	68	Save	read/write
1A	Position Data Ch.7B	read/write	42	TR Ch.2	read/write	6A	Watchdog timer	read/write
1C	Position Data Ch.8A	read/write	44	TR Ch.3	read/write	6C	Soft reset	write
1E	Position Data Ch.8B	read/write	46	TR Ch.4	read/write	6E	Part number	read
20	Wrap-around Ch. 1A	read	48	TR Ch.5	read/write	70	S/N	read
22	Wrap-around Ch. 1B	read	4A	TR Ch.6	read/write	72	Date code	read
24	Wrap-around Ch. 2A	read	4C	TR Ch.7	read/write	74	Rev level	read
26	Wrap-around Ch. 2B	read	4E	TR Ch.8	read/write	76	Outputs, ON/OFF	read/write
						78	Board Ready	read

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Active channels	Ch.8B	Ch.8A	Ch.7B	Ch.7A	Ch.6B	Ch.6A	Ch.5B	Ch.5A	Ch.4B	Ch.3A	Ch.3B	Ch.3A	Ch.2B	Ch.2A	Ch.1B	Ch.1A
2-wire or 3/4-wire	X	X	X	X	X	X	X	X	8A/B	7A/B	6A/B	5A/B	4A/B	3A/B	2A/B	1A/B
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Status, Signal	X	X	X	X	X	X	X	X	8A&B	7A&B	6A&B	5A&B	4A&B	3A&B	2A&B	1A&B
Status, Excitation	X	X	X	X	X	X	X	X	8A&B	7A&B	6A&B	5A&B	4A&B	3A&B	2A&B	1A&B
Status, Test	Ch.8B	Ch.8A	Ch.7B	Ch.7A	Ch.6B	Ch.6A	Ch.5B	Ch.5A	Ch.4B	Ch.3A	Ch.3B	Ch.3A	Ch.2B	Ch.2A	Ch.1B	Ch.1A
Outputs, ON/OFF	1A&B	2A&B	3A&B	4A&B	5A&B	6A&B	7A&B	8A&B	X	X	X	X	X	X	X	X

PROGRAMMING INSTRUCTIONS:

At Power ON or system reset, all parameters are restored to last saved setup and if POST is **enabled,** a D3 test is initiated.

Active channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel register. “1”=active; “0”=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: The current setup can be saved by writing 5555h to the Save register. This register will automatically clear to 00h when the save is completed. (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will.

To restore factory shipped parameters, write AAAAh to the Save register followed by system reset. **Note:** After a Save or Restore, poll the Save register and do not perform any other operation until the Save register is equal to “0”.

Enter Interrupt requirements into the *Interrupt Register* as an 8 bit binary number. 0= no interrupt; 1-7 indicates priority levels.

Any error will latch status register and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, let us consider what happens when a status bit changes before registers are read. For example, if a signal loss was detected and latched into registers and subsequent scans find that the signal was reestablished, then this status change will be held in background until registers are read. After reading, registers will be updated with the background data within 250ms. Allow 250 ms to scan all channels.

Interrupt Vector: Write 16 bit word (0-255) to *Interrupt Vector Register*.

Output ON/OFF: Set the corresponding bit for the channel pair (A and B) to be Enabled or Disabled in the *Output ON/OFF Register*: Factory default is DISABLED

“1” = Output Enabled, “0” = Output Disabled

Example: To enable Channel 1 and disable the rest -> register value = 8000h.

2-wire or 3/4-wire mode: Set the bit corresponding for each output channel pair (A & B) in the *2-3/4 Wire Mode Register*. Setting the bit to “0” => 3/4 wire mode; Setting the bit to “1” => 2 wire mode. When setting a channel pair to 2-wire mode both channels, A & B of that number pair will be set for 2-wire.

Position Output: Enter the position as a 2’s complement number in the corresponding *Position Ch. Data Register* within the range of -1.00 < Position < (+1.00 – lsb). In 3/4-wire mode, position is written only to the A channel of that number pair. The B channel register is ignored. In 2-wire mode the A and B channels are set independently. Factory default: POSITION = 0

Calculate using: register value = POSITION * 32768

Example: For a POSITION = -0.5 -> register value = -0.5 * 32768 = -16384 (0xC000)
Example: For a POSITION = 0.75 -> register value = 0.75 * 32768 = 24576 (0x6000)

The Output voltages in 3/4-wire mode are related to the position by:

Va = Excitation Voltage * TR * [Position/2 + 0.5]

Vb = Excitation Voltage * TR * [1 – (Position/2 + 0.5)]

The Output voltage in 2-wire mode is related to the position by:

V = Excitation Input * TR * Position

Transformation Ratio (TR) for (A&B): Set the TR for the corresponding channel in the *TR Register* using the following formula:

TR register value = TR * 1000

Example: For a TR of 0.5 -> TR register value = 0.5 * 1000 = 500 (0x01F4)
The valid range of TR is: 0.00 <= TR <= 2.00.
NOTE: TR * Input Voltage must be less than 28V
Factory default is TR = 1000 for 1:1.

Optional Excitation Output Voltage: Set the Excitation output voltage in the *Eo Register* using the following formula:

Exc. Out voltage register value = V * 10

Example: For a Excitation output voltage of 7V -> register value = 7 * 10 = 70 (0x0046)
The valid range is: 0.0 <= V <= 28.0

Optional Excitation Output Frequency: Set the Excitation output frequency programmed directly in Hz in the *Eo Register*.

Example: For a Excitation Output Frequency of 1000Hz -> register value = 1000 (0x03E8)
The valid range is: 360 <= F <= 10KHz
It is recommended that user program the required frequency before setting the output voltage.

POST: Will initiate the **D3** test upon Power-On, if POST is enabled and saved. Enable by writing "1" to POST register. Disable, by writing "0" to POST register and then save setup.

Test Enable (D2): Writing "1" to the D2 bit of the *Test Enable Register* initiates automatic background BIT testing that compares the output of each channel with the commanded input to a testing accuracy of 0.2% FS. Results can be read from the Test Status register. A "0" deactivates this test. This test is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. The card will (every 30 seconds) write 55h to the Test (D2) verify register when (D2) is enabled. User can periodically clear to 00h and then after 30 Seconds read the Test (D2) verify register again to verify that background bit testing is activated.

In addition, each Excitation input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Excitation Status Registers*.

Test Enable (D3): Writing "1" to D3 bit of the *Test Enable Register* initiates a BIT test that generates and tests 20 different inputs, to a testing accuracy of 0.2% FS and monitors Excitation and Signal loss. Test cycle takes about 45 seconds and results can be read from *Status Registers.* Excitation is required and outputs must be ON. The testing can be terminated at any time by writing "0" to D3 bit of the *Test Enable Register*. **CAUTION:** During the (D3) test, the outputs are active. Verify that changing those outputs will not effect connected equipment.

To read status: Read the *Signal Status Register* for signal loss, *Excitation Status Register* for excitation loss, and *Test Status Register* for accuracy.
Test: "1" Accuracy OK; "0" failed;
Status: "1" Exc./Sig. On, "0" Exc./Sig. loss.

Read Wrap-Around Angles: Wrap-around positions are read from the *Wrap-around Channel Registers*. Each enabled D/L channel is measured prior to the transformer output and can be read from the corresponding *Wrap-around Channel Register*. The generated result is a 16-bit binary word (or 16-bit 2's compliment word) that represents position. The data is available at any time. **Note:** In 3/4-wire mode, only channels 1-8A need to be read.

Soft reset: (Level sensitive): Writing a "1" to the *Soft Reset Register* initiates and holds software in reset state. Then, writing "0" initiates reboot. It takes 650 ms before card starts initialization sequence and about 15s to complete initialization. This function is equivalent to a power-on reset

Watchdog Timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: Read as a 16 bit binary word from the *Serial Number Register*. This is the serial number of that particular board.

Date Code: Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week).

Revision Level:
Example

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1

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Board Ready: Poll register. Board is ready to be accessed only after you read "AA55." Board is ready approximately 15 seconds after soft reset, or power on.

Front panel Connectors: Mating connectors are not supplied.

J1: DC37P; Mate: DC37S

Pin		Pin		Pin		Pin		Pin	
37	Ch.1 A Lo.	15	Ch.2 B Lo.	29	Exc. Hi 3A-B	24	Ch.5 A Lo.	3	Ch.6 B Lo.
19	Ch.1 A Hi.	33	Ch.2 B Hi.	11	Exc. Lo 3A-B	7	Ch.5 A Hi.	22	Ch.6 B Hi.
18	Ch.1 B Lo.	32	Exc. 2A-B Hi	28	Ch.4 A Lo.	6	Ch.5 B Lo.	2	Exc. 6A-B Hi
36	Ch.1 B Hi.	14	Exc. 2A-B Lo	10	Ch.4 A Hi.	25	Ch.5 B Hi.	20	Exc. 6A-B Lo
35	Exc. 1A-B Hi.	31	Ch.3 A Lo.	9	Ch.4 B Lo.	5	Exc. 5A-B Hi	1	Chassis
17	Exc. 1A-B Lo.	13	Ch.3 A Hi.	27	Ch.4 B Hi.	23	Exc. 5A-B Lo		
34	Ch.2 A Lo.	12	Ch.3 B Lo.	26	Exc. Hi 4A-B	21	Ch.6 A Lo.		
16	Ch.2 A Hi.	30	Ch.3 B Hi.	8	Exc. Lo 4A-B	4	Ch.6 A Hi.		

J2: DC37P; Mate: DC37S

Pin		Pin	
6	Ch.7 A Lo.	31	Ch.8 B Lo.
7	Ch.7 A Hi.	12	Ch.8 B Hi.
27	Ch.7 B Lo.	29	Exc. 8A-B Hi
8	Ch.7 B Hi.	30	Exc. 8A-B Lo
25	Exc. 7A-B Hi.	37	Chassis
26	Exc. 7A-B Lo.	35	Int. Exc. Out Hi
10	Ch.8 A Lo.	17	Int. Exc. Out Lo
11	Ch.8 A Hi.		

P2 Connector:

Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation
18c	Ch.1 A Lo.	32c	Ch.3 A Hi.	12a	Ch.5 B Hi.	29a	Exc. 4A-B Lo	1c	Ch.6 A Lo.	15c	Ch.8 A Hi.
22c	Ch.1 A Hi.	26c	Ch.3 B Hi.	16a	Ch.5 B Lo.	28a	Exc. 5A-B Hi	2c	Ch.6 A Hi.	13c	Ch.8 B Hi.
20c	Ch.1 B Hi.	31c	Ch.3 B Lo.	29c	Exc. 1A-B Hi.	27a	Exc. 5A-B Lo	3c	Ch.6 B Hi.	17c	Ch.8 B Lo.
24c	Ch.1 B Lo.	18a	Ch.4 A Lo.	27c	Exc. 1A-B Lo.	25a	Exc. 6A-B Hi	4c	Ch.6 B Lo.	1d	Internal Exc. Out HI
10c	Ch.2 A Lo.	22a	Ch.4 A Hi.	28c	Exc. 2A-B Hi	26a	Exc. 6A-B Lo	11a	Ch.7 A Lo.	2d	Internal Exc. Out Lo
14c	Ch.2 A Hi.	20a	Ch.4 B Hi.	30c	Exc. 2A-B Lo	19a	Exc. 7A-B Hi	15a	Ch.7 A Hi.		
12c	Ch.2 B Hi.	24a	Ch.4 B Lo.	31a	Exc. 3A-B Hi	23a	Exc. 7A-B Lo	13a	Ch.7 B Hi.		
16c	Ch.2 B Lo.	10a	Ch.5 A Lo.	32a	Exc. 3A-B Lo	19c	Exc. 8A-B Hi	17a	Ch.7 B Lo.		
25c	Ch.3 A Lo.	14a	Ch.5 A Hi.	30a	Exc. 4A-B Hi	21c	Exc. 8A-B Lo	11c	Ch.8 A Lo.		

Do not connect to any undesignated pins.

CODE TABLE

Code	Frequency (I)	Notes
01	400	
02	2.8k – 3.2k	
03	2k	
04	2.69k	
05	1.9k – 2.8k	
06	3k	

Contact factory regarding code list addendum for other operating frequencies/characteristics.

PART NUMBER DESIGNATION

64DL1 - X X X X X X – XX

TOTAL NUMBER OF A & B CHANNELS
2 = 2 Channels*
4 = 4 Channels*
6 = 6 Channels*
8 = 8 Channels*

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

MECHANICAL
F = Front Panel I/O and P2 I/O
P = P2 I/O only
W = P With Wedgelocks
A = VME64 with Blank Front Panel and P2 I/O only
B = VME64 Front Panel with Front Panel I/O & P2 I/O
D = VME64 with Blank Front Panel, Low profile extractors and P2 I/O only

CODE (See Code Table)

OPTIONS
0 = None
9 = Custom Design (See Separate Spec)

EXCITATION INPUTS
C = One Common Input
T = Individual Inputs

EXCITATION SUPPLY
R = On-Board Excitation
E = External Excitation

NOTE:
* Channel density "N" specified for 3 or 4 –Wire Mode. Density doubles to "2N" when using 2-Wire Mode.

Revision Page

Revision	Description of Change	Engineer	Date
5.1	Added Code 7	GS	12/13/01
5.2	Reversed Register Map (76h) Output On/Off to D15-8=Ch1-8, D7-0=x (Don't care) For 2-wire config., only 8 channels are available (not 16). Memory Map: 5Ah is read only, 58h is Interrupt Level. Output format of this card can be wired (not configured).	GS	12/14/01
5.3	Memory Map 0x00->0x1c are Ch's 1-8; Corrected J1 conn. pinout Ch6 Label "A" side.	GS	12/20/01
5.4	Description, line 1, "sixteen" is actually "eight" (8) two-wire...	GS	01/04/02
5.5	See code list addendum for descriptions of code 50 and above. Part Number: contact factory for other temperature requirements. Removed temp "M". Non-volatile, not permanent memory. Save is R/W.	GS	02/06/02
5.6	Removed Part Number "L" Option, VME64 front panel with Low profile extractors and with front panel I/O & P2 I/O. Front panel I/O interferes with extractors.	GS	06/19/02
5.7	Update LARGE DL Graphic	GS	06/27/02
5.8	Correct Polarity in Diagrams for Principles of LVDT Operation	GS	06/28/02
5.9	Standardized PN, Mech. Options List to FPWABD. Added support for 2 Wire mode: B Position Data and Wrap Around Registers as well as their function descriptions. Added Board Ready register. B channel support is provided with new mother-board DS1 rev D – almost considered model DS3/DL3.	GS	07/30/02
6.0	Added codes 5 and 6 (removed 7 as it is the same as 5 (see master code list)	GS	08/13/02
6.1	Read Wrap: In 3/4-wire mode, only channels 1-8A (not 1-6A) need to be read. Transformer Ration: TR register value = 0.5 * 1000 (not 100)	GS	10/22/02
6.2	Added Board Ready & Rev description. Removed Factory default from ¾-2 wire mode. Change TR default from 0 to 1000 (1:1). Deleted default from Ref Volt and frequency. Added "It takes 650ms before care starts initialization sequence and about 15s to complete initialization." To Soft reset description	GS	10/25/02
6.3	Only for clarity, Va = Excitation Voltage * TR * [Position/2 + 0.5], Vb = Excitation Voltage * TR * [1 – (Position/2 + 0.5)]	GS	02/05/03
6.4	Adds Output Voltage (+- 24 volt) spec., Corrects BIT Bit-Map.	GS	07/22/03
6.5	FOR COMMERCIAL AND MILITARY APPLICATIONS. Reference spec calls out 2-28V (not 115).	GS	08/08/05
6.6	Corrected drawings in Principal of Operation LVDT (pg 2)	FH / ars	11/03/05
6.7	Corrected "typo" P2 connector pinout; 19c, 21c, 17c	FH / ars	12/05/05
6.8	New Address	KL	04/24/07
6.9	Clarified address byte boundaries: from 256 to 512 byte boundaries; legacy cards DOM 0848 and earlier were 256 byte boundaries (pg. 3); Agile release.	AS	05/19/10