Eight (8) S/D and Six (6) D/S (1.2 VA)

Single Speed or Two-Speed (for both S/D & D/S), Programmable
Multi-Speed Ratios: 2 to 255
Accurate Velocity Outputs; D/S Rotation, Continuous Self-Test;
On-Board Programmable Reference Supply (Optional)

FEATURES:

- 16 bit resolution
- 1 arc minute accuracy for measurement channels; 30 arc seconds accuracy for stimulus channels
- Continuous background bit testing with Reference and Signal loss detection
- Power-On Self-Test (POST)
- **S/D channels are self-calibrating**
- **Automatically supports either 5V or 3.3V PCI bus**
- 47 Hz to 10 kHz Variations available
- Encoder (A & B) plus Index Outputs with Programmable resolution-Optional
- Synchro/Resolver Programmable-Optional (Measurement side S/D)
- ON/OFF for D/S channels
- Transformer isolated
- Accurate Digital Velocity outputs
- Latch feature
- Synthetic reference for S/D compensates for ±60° phase shift
- No adjustments or trimming required
- Part number, S/N, Date code, & Rev. in non-volatile memory

DESCRIPTION:

This single slot card contains **separate transformer isolated Synchro/Resolver-to-Digital tracking converters, separate transformer isolated Digital-to-Synchro/Resolver converters (1.2 VA), optional internal 5 VA reference, and extensive diagnostics. The maximum channel density of the card is fixed at: 8 S/D (maximum measurement applications) with 6 D/S (for maximum stimulus applications). Variations of S/D and D/S channels can be specified as shown in the Part Number Designation at the end of this specification. The measurement channels incorporate Synchro/Resolver inputs, high linearity digital velocity outputs, angle change alert and ability to field configure for either single speed or multi-speed to any ratio between 2 and 255. The Stimulus channels include ON/OFF capability, individual reference inputs are supplied for each channel, two-speed programmability, and rotation with start and stop angles.** The S/D channels, even when large accelerations are encountered, never lose tracking, because they incorporate the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. The “Latch” feature permits the user to read all channels at the same time. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified tracking rate. A step input will not cause any hang-up condition. Intermediate transparent latches, assure that current valid data is always available for any channel without effecting the tracking performance of the converters. For two-speed applications, our ambiguity circuits maintain monotonic outputs by compensating for variations of the zero positions between the Coarse and Fine Synchros. However, if the maximum allowable angle difference of 90°/n is exceeded, a flag will be set that indicates to the user that the input Synchro’s are out of alignment. The Stimulus channels offer short circuit protection and the ability to ground one of the outputs without effecting performance. External amplifiers can be added to drive up to 30 watts with a frequency range of 50 to 400 Hz. Customized output voltages can be supplied for the D/S channels to minimize the need for multiple cards because Resolver outputs are not standardized. (Contact factory for information). Each channel can be

specified for a different voltage and frequency. To simplify logistics, Part number, S/N, Date code, & Rev. are located in non-volatile memory locations.

Major diagnostics are incorporated that offer substantial improvements to system reliability because user is immediately alerted to channel malfunctions. This approach also reduces bus traffic because the *Status Registers* do not require constant polling. Power-On, Self-Test (POST) diagnostic can immediately initiate (D3) test.
See Programming Instructions for further details.

Three different tests (one on-line and two off-line) can be selected:
The (D2) test for measurement channels initiates automatic background bit testing. Each channel is checked every 5° to a test accuracy of 0.05°. Any failure triggers an Interrupt (if enabled) and the results are available in the *S/D Test Status Registers*. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the S/D *Signal* and *Reference Status Registers*.

The (D2) Test for stimulus channels initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the *commanded angle*. The status bits will be set to indicate an accuracy problem and the results can be read from *D/S Test Status Register*.

In addition, each D/S Reference input and Signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the D/S Signal and Reference status registers.

The (D3) or POST test for measurement channels, (if enabled), is an initiated bit test that disconnects all input channels from the outside and connects them across internal test signals that generate and test 72 different angles to a test accuracy of 0.05°. External reference is required for the D/S channels. Any failure triggers an Interrupt (if enabled). Testing requires no external programming, and can be enabled or disabled via the bus.

The (D3) or POST test for stimulus channels, starts a BIT Test that generates and tests 72 different angles, to a testing accuracy of 0.05°. Results can be read from Status Registers. External reference is required. Testing requires no external programming, and can be Initiated or terminated via the bus. **CAUTION: Outputs are active during this test**. Check connected loads for possible interaction.

The (D0) test is used to check the card and the interface. All input channels are disconnected from the outside and connected across the internal test signals, thus allowing user to write any angle to the card and then read the data from the interface. D/S outputs are programmed the same as for normal operation. External reference required only for D/S.

NOTE: ALL D/S TESTS REQUIRE THE OUTPUTS TO BE "ON" AND THAT A REFERENCE IS SUPPLIED.

SPECIFICATIONS:	Applies to each Measurement channel
Resolution:	16 bit (Up to 24 bit for two-speed mode)
Accuracy:	±1 arc minute for single speed inputs (±1 arc minute divided by gear ratio for two-speed)
Tracking Rate:	18.5 RPS for 60 Hz version; 150 RPS for 360 Hz or greater versions. (Referred to the Fine input for two-speed configuration)
Bandwidth:	10 Hz for 60 Hz versions; 40 Hz for 400 Hz versions, & 100 Hz for greater than 1 kHz version. (also can be factory customized)
Input format:	Synchro or Resolver, (See part number)
Input voltage:	Resolver : 2-28 V_{L-L} Autoranging, or 90 V_{L-L} Synchro : 11.8 V_{L-L} , or 90 V_{L-L} Resolver and Synchro are transformer isolated Other input options available; consult factory.
Input Impedance:	26 V_{L-L} or less: 40 kΩ min. 90 V_{L-L}: 100 kΩ min.
Reference/Input:	2-115 Vrms, @ 5 ma max ; Transformer isolated. (See part number)
Frequency:	47 Hz to 10 kHz (See part number)
Encoder outputs:	Either 12,13,14,15, or 16-bit resolution, (field programmable) with Index marker. 12-bit resolution is equivalent to 1,024 cycles (4,096 transitions), 13-bit is 2,048 cycles (8,192 transitions) etc. After the encoder resolution has been selected, (12-16 Bits), it will not change with varying input speeds. Differential outputs are complementary TTL (use TTL+ and dc gnd for short distances or TTL(+) and (–) in the differential mode, into differential receivers for long distance to avoid ground noise). Optional, see P/N.
Commutation outputs:	Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors

Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°
Velocity, Digital:	16 bit resolution; Linearity: 0.1%
Two-speed ratio:	Programmable from 2 to 255.
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt is generated. Default is disabled. Msb = 180°; Minimum differential is 0.05°. Max differential that can be programmed is 179.9°.

SPECIFICATIONS

Applies to each Stimulus Channel

Resolution:	16 bits (.0055°)
Accuracy:	30 arc seconds (.008°) at 0.3 VA ±1 arc minute (.017°) at 1.2 VA. No load to full load
Two-Speed ratio:	Programmable from 2 to 255.
Rotation:	Programmable Start and Stop angles. 0 rps to ±13.5 rps with a resolution of 0.15°/sec. Stepping rate is 16 bits to 3.4 rps, then is automatically reduced to 14 bits up to 13.5 rps.
Output format:	Synchro or Resolver, (See part number), transformer isolated
Output voltage:	2-90 VL-L (See part number).
Output load:	1.2 VA max./Channel. Short circuit protected (5000 Ω reactive at 90 VL-L; Synchro, 90 Ω reactive at 11.8 Synchro, 110 Ω reactive at 11.8 VL-L Resolver)
Regulation:	5% max. No load to Full load
Reference voltage:	2-26VAC, 115VAC (See part number), transformer isolated.
Reference frequency:	47 Hz to 10 kHz (See part number). 47 Hz for use with external amplifiers
Reference current:	1 ma max./Channel
Phase shift:	5° max. between output and reference.
Settling time:	Less than 100 microseconds

REFERENCE SUPPLY:

Optional. (See part number).

Voltage:	2.0-28Vrms programmable, resolution 0.1Vrms, or 115Vrms fixed. Accuracy ±2%
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 190mA RMS @ 2-26VAC, 45mA RMS @ 115VAC Note: Power is reduced linearly as the Reference Voltage.

GENERAL SPECIFICATIONS:

Signal Logic Level:	Automatically supports either 5V or 3.3V PCI bus.	
Power:	See current requirement Table 1 below. Power supplies must be able to supply the peak power without current limiting.	
Temperature, operating:	"C" = 0°C to +70°C, "E" = -40°C to +85°C (See part number)	
Temperature, storage:	-55° C to +105° C	
Size:	3.950 (10.033) height, 12.285 (31.204) length; less front panel connector J1; dimensioned in inches (cm)	
Weight:	Board & heat sink less modules	10 oz. Max.
	S/D modules @ 4 Ch ea.	2.5 oz. Max.
	D/S modules w/ transformers 2Ch ea.	5.0 oz. Max.
	Reference module	1.8 oz. Max.

CURRENT REQUIREMENTS:

	±12Vdc	+5Vdc
Board – no Modules	15mA	460mA
Add per 4 Ch S/D Mod	15mA	160mA
Add per 2 Ch D/S Mod	140mA	35mA
Add per 1.2 VA Load	125mA (400mA Peak)	
Reference Module		1A @ 5VA Load (3A Peak)

TABLE 1

000	S/D Ch.1 Data	read	0A4	Power-On (POST) enable **S/D**	read/write	148	Stop angle Ch.3	read/write
004	S/D Ch.2 Data Hi [1]	read	0A8	Lock loss	read	14C	Stop angle Ch.4	read/write
008	S/D Ch.3 Data	read	0AC	(A&B) resolution/poles Ch. 1	read/write	150	Stop angle Ch.5	read/write
00C	S/D Ch.4 Data Hi [1]	read	0B0	(A&B) resolution/poles Ch. 2	read/write	154	Stop angle Ch.6	read/write
010	S/D Ch.5 Data	read	0B4	(A&B) resolution/poles Ch. 3	read/write	158	Rotation rate, D/S Ch.1	read/write
014	S/D Ch.6 Data Hi [1]	read	0B8	(A&B) resolution/poles Ch. 4	read/write	15C	Rotation rate, D/S Ch.2	read/write
018	S/D Ch.7 Data	read	0BC	(A&B) resolution/poles Ch. 5	read/write	160	Rotation rate, D/S Ch.3	read/write
01C	S/D Ch.8 Data Hi [1]	read	0C0	(A&B) resolution/poles Ch. 6	read/write	164	Rotation rate, D/S Ch.4	read/write
020	Velocity, S/D Ch.1	read	0C4	(A&B) resolution/poles Ch. 7	read/write	168	Rotation rate, D/S Ch.5	read/write
024	Velocity, S/D Ch.2	read	0C8	(A&B) resolution/poles Ch. 8	read/write	16C	Rotation rate, D/S Ch.6	read/write
028	Velocity, S/D Ch.3	read	0CC	Velocity, S/D scale Ch.1	read/write	170	Rotation, Initiate	write
02C	Velocity, S/D Ch.4	read	0D0	Velocity, S/D scale Ch.2	read/write	174	Rotation, Stop	write
030	Velocity, S/D Ch.5	read	0D4	Velocity, S/D scale Ch.3	read/write	178	Rotation Mode	read/write
034	Velocity, S/D Ch.6	read	0D8	Velocity, S/D scale Ch.4	read/write	17C	*Rotation completed N/A* [2]	*read*
038	Velocity, S/D Ch.7	read	0DC	Velocity, S/D scale Ch.5	read/write	180	Status, Signal **D/S**	read
03C	Velocity, S/D Ch.8	read	0E0	Velocity, S/D scale Ch.6	read/write	184	Status, Reference **D/S**	read
040	Ratio S/D Ch.1/2	read/write	0E4	Velocity, S/D scale Ch.7	read/write	188	Status, Test **D/S**	read
044	Ratio S/D Ch.3/4	read/write	0E8	Velocity, S/D scale Ch.8	read/write	190	Test (D2) verify, **D/S**	read/write
048	Ratio S/D Ch.5/6	read/write	0F0	S/D Ch.2 Data Lo [1]	read	194	Test Enable, **D/S**	read/write
04C	Ratio S/D Ch.7/8	read/write	0F4	S/D Ch.4 Data Lo [1]	read	198	Power-On (POST) enable **D/S**	read/write
050	Angle Δ Ch.1	read/write	0F8	S/D Ch.6 Data Lo [1]	read	1A0	Active channels, **D/S**	read/write
054	Angle Δ Ch.2	read/write	0FC	S/D Ch.8 Data Lo [1]	read	1A4	Outputs ON/OFF	read/write
058	Angle Δ Ch.3	read/write	100	D/S Ch.1 Data	read/write	1B0	Interrupt Enable	read/write
05C	Angle Δ Ch.4	read/write	104	D/S Ch.2 Data	read/write	1B4	Interrupt Status	read
060	Angle Δ Ch.5	read/write	108	D/S Ch.3 Data	read/write	1B8	Freq. (Ref. Supply)	read/write
064	Angle Δ Ch.6	read/write	10C	D/S Ch.4 Data	read/write	1BC	Voltage (Ref. Supply)	read/write
068	Angle Δ Ch.7	read/write	110	D/S Ch.5 Data	read/write	1C0	Watchdog timer	read/write
06C	Angle Δ Ch.8	read/write	114	D/S Ch.6 Data	read/write	1C4	Soft reset	write
070	Angle Δ initiate	write	118	Wrap-around D/S Ch.1	read	1C8	Part #	read
074	Active channels, **S/D**	read/write	11C	Wrap-around D/S Ch.2	read	1CC	Serial #	read
078	Test (D2) verify, **S/D**	read/write	120	Wrap-around D/S Ch.3	read	1D0	Date code	read
07C	Test Enable, **S/D**	read/write	124	Wrap-around D/S Ch.4	read	1D4	Rev level PCB	read
080	Status, Signal **S/D**	read	128	Wrap-around D/S Ch.5	read	1D8	Rev. level S/D DSP	read
084	Status, Reference **S/D**	read	12C	Wrap-around D/S Ch.6	read	1DC	Rev. level S/D FPGA	read
088	Status, Test **S/D**	read	130	Ratio, D/S Ch.1/2	read/write	1E0	Rev. level D/S DSP	read
08C	Latch	write	134	Ratio, D/S Ch.3/4	read/write	1E4	Rev. level D/S FPGA	read
090	S/D Test angle	read/write	138	Ratio, D/S Ch.5/6	read/write	1EC	Rev. level Interface FPGA	read
094	Angle Δ alert	read	140	Stop angle Ch.1	read/write	1FC	Save	read/write
0A0	Synchro/Resolver	read/write	144	Stop angle Ch.2	read/write			

TABLE 2

Note 1 – Read channels (2,4,6,8,etc.) for combined 16-bit output. For 24 bit resolution, read Lo then Hi word. When read, Lo word latches Hi word.

Note 2 – Currently Not Implemented

Register Bit Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data (angle)° Hi [1]	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Data (angle)° Lo [1]	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	0	0	0	0	0	0	0	0
Active channels, **D/S**	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
D/S outputs ON/OFF	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Rotation Mode	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Rotation, Initiate	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Rotation, Stop	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Rotation completed	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Rotation, Start/Stop	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Test Enable, **D/S**	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Status, Test **D/S**	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Status, Signal **D/S**	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Status, Reference **D/S**	X	X	X	X	X	X	X	X	X	X	DS6	DS5	DS4	DS3	DS2	DS1
Active channels, **S/D**	X	X	X	X	X	X	X	X	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Latch outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Two-speed lock loss	X	X	X	X	X	X	X	X	Ch7/8	X	Ch5/6	X	Ch3/4	X	Ch1/2	X
Synchro/Resolver	X	X	X	X	X	X	X	X	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Test Enable, **S/D**	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Status, Test **S/D**	X	X	X	X	X	X	X	X	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Status, Signal **S/D**	X	X	X	X	X	X	X	X	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Status, Reference **S/D**	X	X	X	X	X	X	X	X	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Angle Δ Alert **S/D**	X	X	X	X	X	X	X	X	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1
Interrupt Enable/Status	X	X	X	X	X	#7	#6	#5	X	X	X	X	#4	#3	#2	#1
(A&B) resolution/poles	D15	X	X	X	X	X	X	X	X	X	X	X	X	**D2**	**D1**	**D0**

↑ "0"= Encoder
"1"= Commutation

TABLE 3

		D2	D1	D0
4 pole	**16 bit**	0	0	0
6 pole	**15 bit**	0	0	1
8 pole	**14 bit**	0	1	0
↑	**13 bit**	0	1	1
	12 bit	1	0	0

Commutation outputs ↑

Encoder outputs ↑

Note 1 –Values are rounded off.

INTERRUPT ENABLE & STATUS REGISTERS

#1 = S/D Signal Loss
#2 = S/D Reference Loss
#3 = S/D Angle Change Alert (Global – Read *Angle Change Alert Register* for particular channel failure)
#4 = S/D Test Accuracy Error
#5 = D/S Signal Loss
#6 = D/S Reference Loss
#7 = D/S Test Accuracy Error

Measurement (S/D) Specific Registers

S/D Active Channels: Set the bit corresponding to each channel to be monitored during BIT testing in the S/D *Active Channel Register* ("1"=active; "0"=not used). **Omitting this step will produce errors on unused channels causing false alarms**; hence unused channels will set faults, i.e. status bits, interrupts, etc.

Save Setup: Writing 5555h to the *Save Register* will save the current setup. This location will automatically clear to 0000h when save is completed (within 5 seconds). When save is elected, all parameters are saved. However, any parameter can be changed at any time. Saving is optional. If not saved, reenter parameters at each Power-On. To restore factory shipped parameters, write AAAAh to the *Save Register*, followed by System Reset. Note: After a SAVE or RESTORE, poll the *Save Register* and **do not perform any operation until word is at 0000h.**

Optional Synchro/Resolver Mode: Where applicable, write a "1" or "0" (Synchro = 1; Resolver = 0) to each bit, representing a channel, of *Synchro/Resolver Register*.

S/D Ratio: Enter the desired ratio, as an integer number, in the *S/D Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Read: For single speed applications (Ratio=1), read individual channels 1,2,3,4,etc. For two-speed applications, read only channels (2,4,6,8,etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word.

In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4, CH5 & 6, or CH7 & 8.

Two-Speed Lock-Loss: The card monitors misalignment between Coarse and Fine angles during two-speed operation. A two-speed lock loss condition exists if the maximum allowable misalignment between the Coarse and Fine angles of 90°/ratio is exceeded. The corresponding bit for that channel pair in the *Two-Speed Lock-Loss Register* will be set to "0".

Latch: Writing the integer 2 to the *Latch Register* will cause the angle data of all channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing 0 to this register will disengage latch on all channels.

Velocity Output: Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then
Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

Velocity Scale Factor: The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec resolution (lowest setting)

S/D Power-On Self-Test (POST): The unit will initiate the D3 Test upon power-on, if POST is enabled and saved. Enable by writing "1" to *POST Register*. Disable by writing "0" to *POST Register* and then save setup.

S/D D2 Test Enable: Writing "1" to the D2 bit of the *S/D Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. The result of an accuracy error is available in the *S/D Test Status Register* and if enabled, an interrupt will be generated (See *Interrupt Register*). A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. The card will write 55h to the *S/D Test (D2) Verify Register*, every 30 seconds, when the D2 Test is enabled. User can periodically clear the *Test (D2) Verify Register* by writing 00h, waiting 30 seconds, then reading the register again to verify that background BIT testing is activated.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *S/D Signal* and *Reference Status Registers*.

S/D D3 Test Enable: Writing "1" to the D3 bit of the *S/D Test Enable Register* initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. The test cycle is completed within 45 seconds and results can be read from the *S/D Test Status Registers* when D3 bit changes from "1" to "0" and if enabled, an interrupt will be generated if a BIT failure is detected (See *Interrupt Register*). The testing can be terminated at any time by writing "0" to D3 bit of the *S/D Test Enable Register*.

Signal and Reference monitoring is disabled during D3 test.

S/D D0 Test Enable: Used to check card and PC interface. Writing "1" to the D0 bit of the *S/D Test Enable Register* disconnects all channels from the outside world and connects them to internal test signals, enabling the user to generate any test angle by writing an integer value, to the *S/D Test Angle Register*. Data is then read through the interface (after writing, allow 400 ms before reading). External reference is not required. (e.g. 330° = angle/(360/2^{16})).

Signal and Reference monitoring is disabled during D0 test.

S/D Status, Test: Check the channel's corresponding bit of the *S/D Test Status Register* for status of BIT testing for each active channel. A "1" means accuracy passes; A "0" indicates a failure on an active channel. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any S/D Test status failure, transient or intermittent will latch the *S/D Test Status Register*. Reading will unlatch register.

S/D Status, Reference: Check the channel's corresponding bit of the *S/D Reference Status Register* for status of the reference input for each active channel. A "1" means Reference ON, a "0" means Reference Loss on active channels. Channels that are inactive are also set to "0". (Reference loss is detected within 2 seconds). Reference monitoring is disabled during D3 or D0 Test. Any S/D Reference status failure, transient or intermittent will latch the *S/D Reference Status Register*. Reading will unlatch register.

S/D Status, Signal: Check the corresponding bit of the *S/D Signal Status Register* for status of the input signals for each active channel. A "1" means Signal is valid (level must be a minimum of 2V), a "0" means Signal loss on active channels. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Signal monitoring is disabled during D3 and D0 test. Channels that are inactive are also set to "0". Any S/D Signal status failure, transient or intermittent will latch the *S/D Signal Status Register*. Reading will unlatch register.

Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. After reading, registers will be updated with the background data within 250ms. Allow 250 ms to scan all channels.

Angle Change Alert: Write a 16-bit word to the appropriate *Angle Change Register* for a given channel, to represent the minimum differential change required. MSB=180°; Minimum differential is 0.05°, setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring by writing "1" to *Angle Change Initiate Register*.

When that differential is exceeded, on any monitored channel, the bit corresponding to that channel is set in *Angle Change Alert Register* ("0" = no change, "1" = change).

Optional (A&B) Encoder Resolution: To set Encoder Mode, write a "0" to the D15 bit and the appropriate code for the desired resolution to the D2, D1 & D0 bits of the corresponding channel *(A&B) Resolution/Poles Register*. Changing the resolution for any channel can be done on the fly. The default is a 12bit resolution encoder output. See Table 3.
Note: Encoder/Commutation outputs are optional; see part ordering information.

Optional Commutation Outputs (A,B,C): To set Commutation Mode, write a "1" to the D15 bit and the appropriate code for the required motor poles to the D2, D1 & D0 bits of the corresponding channel *(A&B) Resolution/Poles Register*. See Register Bit map table.
Note: Encoder/Commutation outputs are optional; see part ordering information.

Stimulus D/S Specific Registers

D/S Active Channels: Set the bit corresponding to each channel to be monitored during BIT testing in the D/S *Active Channel Register* ("1"=active; "0"=not used). **Omitting this step will produce errors on unused channels causing false alarms**; hence unused channels will set faults, i.e. status bits, interrupts, etc.

Write Angle – Single Speed:

For single-speed applications (Ratio=1), write a 16-bit integer (or 16-bit 2's compliment integer) to the corresponding channel *D/S Data Register.* (ex. 330° = EAABh).
WORD = (Angle ÷ (360/2^{16})).
Note: writing to an Input Angle Register will stop any rotation initiated on that channel

Write Angle – Two-Speed:

In two-speed applications, the ratio will affect the fine speed output resolution. (Higher ratios result in lower resolutions at the output.) This occurs from multiplying the coarse angle by the ratio to achieve the fine angle output. This multiply reduces the overall resolution by increasing the weight of the LSB's. To compensate for

this, the card allows for 24-bit resolution for the higher ratios. This feature is transparent and automatic to the user and will regain the resolution needed in higher ratio systems.

When 16 bit resolution is sufficient, the angle can be represented by first writing the integer 0 to the even channel of the pair *D/S Data Register,* then a 16-bit integer (or 16-bit 2's compliment integer) to the odd channel of the pair (coarse speed) *D/S Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. Note: Integer 0 only needs to be written to the even channel once to initialize the even channel register. Subsequently, only writes to the odd channel are necessary.

Odd Channel	Even Channel
16 Bits	0

16 bit integer = Angle / $(360/2^{16})$; Fine Speed ≡ Angle * Ratio / $(360/2^{16})$

Ex1. For a ratio of 255, the fine speed output would have a resolution of 1.4008°.
Thus, for every 0.00549° of shaft angle, the fine output will change in 1.4008° increments.

When 24 bit resolution is desired, the angle can be represented as a 24-bit integer (or 24-bit 2's compliment integer) by first writing the lower 8-bits to the upper byte of the even channel of the pair of the *D/S Data Register*, then the upper 16-bits to the odd channel of the pair (coarse speed) of the *D/S Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. The channel pairs are defined as Ch1&2, Ch3&4, Ch5&6 and Ch7&8.

Odd Channel	Even Channel	
16 Bits	8 Bits	X

24 bit integer = Angle / $(360/2^{24})$; Fine Speed ≡ Angle * Ratio / $(360/2^{24})$

Ex1. For a ratio of 255, the fine speed output would have a resolution of 0.00547°.
Thus, for every 0.000021458° of shaft angle, the fine output will change in 0.00547° increments.

Note: Writing to an input angle register will stop any rotation initiated on that channel.

D/S Ratio: Enter the desired ratio, as an integer number, in the *D/S Ratio Register* corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Outputs ON/OFF: Set the bit corresponding to each channel to be turned on, to "1" in the *Output On/Off Register*. To turn OFF a channel, set corresponding bit to "0". Default: Set to OFF

Read Wrap-Around Angles: Wrap-around angles are read from the *D/S Wrap-around Registers*. Each enabled D/S channel is measured prior to the transformer output and can be read from the corresponding *D/S Wrap-around Register*. The generated result is a 16-bit binary word (or 16-bit 2's compliment word). The data is available at any time.

Rotation Rate: Write a 2's compliment number representing the desired rotation rate, to the corresponding *Rotation Rate Register*. LSB = 0.15°/sec.
Ex: 12 RPS = (12 x (360°/0.15°) = 28800 (7080h), -12 RPS = (-12 x (360°/0.15°) = -28800 (8F80h).
Stepping rate is 16 bits (0.0055°) for up to 3.4 RPS, then linearly decreases to 14 bits (0.022°) at 13.5 RPS.

Rotation Mode, Continuous or Start/Stop: For continuous rotation, set the corresponding channel bit to "0" in the *Rotation Mode Register*. For rotation to cease at a designated stop angle, set the bit to "1".

Stop Angles: Write the desired stop angle to appropriate channel *Stop Angle Register*. After a channel reaches the stop angle, it will stop rotating and remain at that angle until a new input angle is set. If rotation is initiated again, the angle will start rotating from the present angle.

Initiate Rotation: First set the *Rotation Rate* and *Rotation Mode Register* for each channel that is to rotate. Then, to start rotation for those channels, set the corresponding channel bit to a "1" in the *Rotation Initiate Register*.

Stop Rotation: Set the corresponding bit, for each channel to be stopped, to a "1" in the *Rotation Stop Register*. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated.

Rotation Completed: (not implemented - consult factory) *Read the Rotation Completed Register. Each bit corresponds to a given channel. A "1" = rotation completed, "0"=rotation in process.*

D/S Power-On Self-Test (POST): The unit will initiate the D3 Test on Power-On, if POST is enabled and saved. Enable by writing "1" or Disable by writing "0" to *POST Register* and then save setup.

D/S D2 Test Enable: Writing "1" to the D2 bit of the *D/S Test Enable Register* initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before

the output transformer, to the commanded angle. The status bits will be set to indicate an accuracy (0.05º) problem and the results can be read from *D/S Status Registers* within 2 seconds and if enabled, an interrupt will be generated (See *Interrupt Register*. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Outputs must be ON and Reference supplied for test to function. Card will write 55h (every 2 seconds) to the *D/S Test (D2) Verify Register* when D2 is enabled. User can periodically clear to 00h and then read the *D/S Test (D2) Verify Register* again, after 2 seconds, to verify that BIT Testing is activated. This test continuously sequences between the six channels on the card with each output being measured for approx. 180mSec. If the measured angle has an error greater the 0.05º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *D/S Signal* and *D/S Reference Status Registers*.

D/S D3 Test Enable: Writing "1" to the D3 bit of the *D/S Test Enable Register* initiates a BIT Test that generates and tests 72 different angles to an accuracy of 0.05°. External reference is required and outputs must be ON. The D/S Status bits will be set to indicate an accuracy problem. Results are available in the *D/S Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 30 seconds and the D3 bit changes from "1" to "0" when test is complete. The testing requires no external programming, and can be terminated at any time by writing a "0" to the D3 bit of the *D/S Test Enable Register*. **CAUTION: Outputs must be ON and Reference supplied during this test and is therefore active.** Check connected loads for possible interaction.

D/S Status, Test: Check the corresponding bit of the *D/S Test Status Register* for status of BIT Testing for each active channel. A "1" means Accuracy OK; "0" failed. Channels that are inactive are also set to "0". (test cycle takes 2 seconds for accuracy error). Any D/S Test status failure, transient or intermittent will latch the *D/S Test Status Register*. Reading will unlatch register.

D/S Status, Ref: Check the corresponding bit of the *D/S Reference Status Register* for status of the reference input for each active channel. A "1" means Reference ON, "0" means Reference Loss on active channels. Channels that are inactive are also set to "0". (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any D/S Reference status failure, transient or intermittent will latch the *D/S Reference Status Register*. Reading will unlatch register.

D/S Status, Sig: Check the corresponding bit of the *D/S Signal Status Register* for status of the output signals for each active channel. A "1" means Signal is valid, "0" means Signal loss. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Signal monitoring is always enabled. Any D/S Signal status failure, transient or intermittent will latch the *D/S Signal Status Register*. Reading will unlatch register.

General User Registers

Power On Reset or System Reset: All parameters are restored to last saved setup and, if POST was previously enabled in last setup, a D3 Test will be initiated. A power on automatic calibration test is run and completes in approximately 30 seconds.

Interrupt Registers: Interrupts can be enabled to relay specific problems/failures detected by the card. The problem/failures that generate these interrupts are:

S/D Signal Loss, S/D Reference Loss, S/D Angle Change Alert, S/D Test Accuracy Error,
D/S Signal Loss, D/S Reference Loss & D/S Test Accuracy Error

Each external interrupt can be enabled individually. This is accomplished by writing a "1" to the bit corresponding to desired interrupts to the *Interrupt Enable Register* and a "0" to disable those interrupts not used. Refer to Table 3.

Interrupt Status Registers: When an interrupt is initiated via a problem/failure, the *Interrupt Status Register* can be interrogated by a read to identify, which interrupt occurred. Refer to Table 3. Register is latched when interrupt is generated and unlatched when read.

Note: This register is typically read and cleared by the device driver. Subsequent readings of this register will give clear status.

Optional Reference Supply: For frequency, write a 16-bit integer to the *Frequency Ref Supply Register*. (Ex: 400 Hz = 0190h) with LSB= 1Hz. For voltage, write a 16-bit integer to the *Voltage Ref Supply Register*. (Ex: 26Vrms =0104h) with LSB=0.1Vrms. It is recommended that the user program the required frequency before setting the output voltage.

Soft Reset: Write an integer "1" to *Soft Reset Register*, then clear to 0 before 50ms elapses. **CAUTION: Register is level sensitive and for proper card operation, the logic level "1", or pulsewidth, must be <= 50ms**. Considering minimum and maximum, 1 µs < pulsewidth <= 50ms. Processor reboots in about 400 ms, after which calibration procedures begin. This function is equivalent to a power-on reset.

Watchdog Timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: Read as a 16-bit binary word from the *Serial Number Register*. This is the serial number of that particular board.

Date Code: Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week)

Rev Levels: There are a total of 6 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Rev level PCB
Rev level S/D DSP
Rev level S/D FPGA
Rev level D/S DSP
Rev level D/S FPGA
Rev level Interface FPGA

Software - PCI Programming

This section provides programmers the information needed for developing drivers other than those supplied.

The following information resides in the PCI configuration registers:

Device ID	= 7621	(hex)
Vendor ID	= 15AC	(hex)
Rev	= 01	(hex)
Subsystem ID	= 000115AC	(hex)

Base Address = Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information.
Required Address space = 1K for each card.

EXTERNAL +/- 12VDC: (JP6 & JP7)

The card is shipped and configured for operation with +/- 12 VDC power, being supplied from edge connector.

To operate from External +/- 12VDC supplies: On jumper block JP7, remove jumpers 1-2, and 5-6, then re-connect jumpers 3-4 and 7-8. Leave jumper 9 – 10 connected.

Connect external +12 VDC to JP6-4, connect external –12 VDC to JP6-2 and external ground to JP6-1**.**

Pin JP6-3 has been removed for keying. We recommend customer plug receptacle pin 3 to insure proper connection and avoid damage.

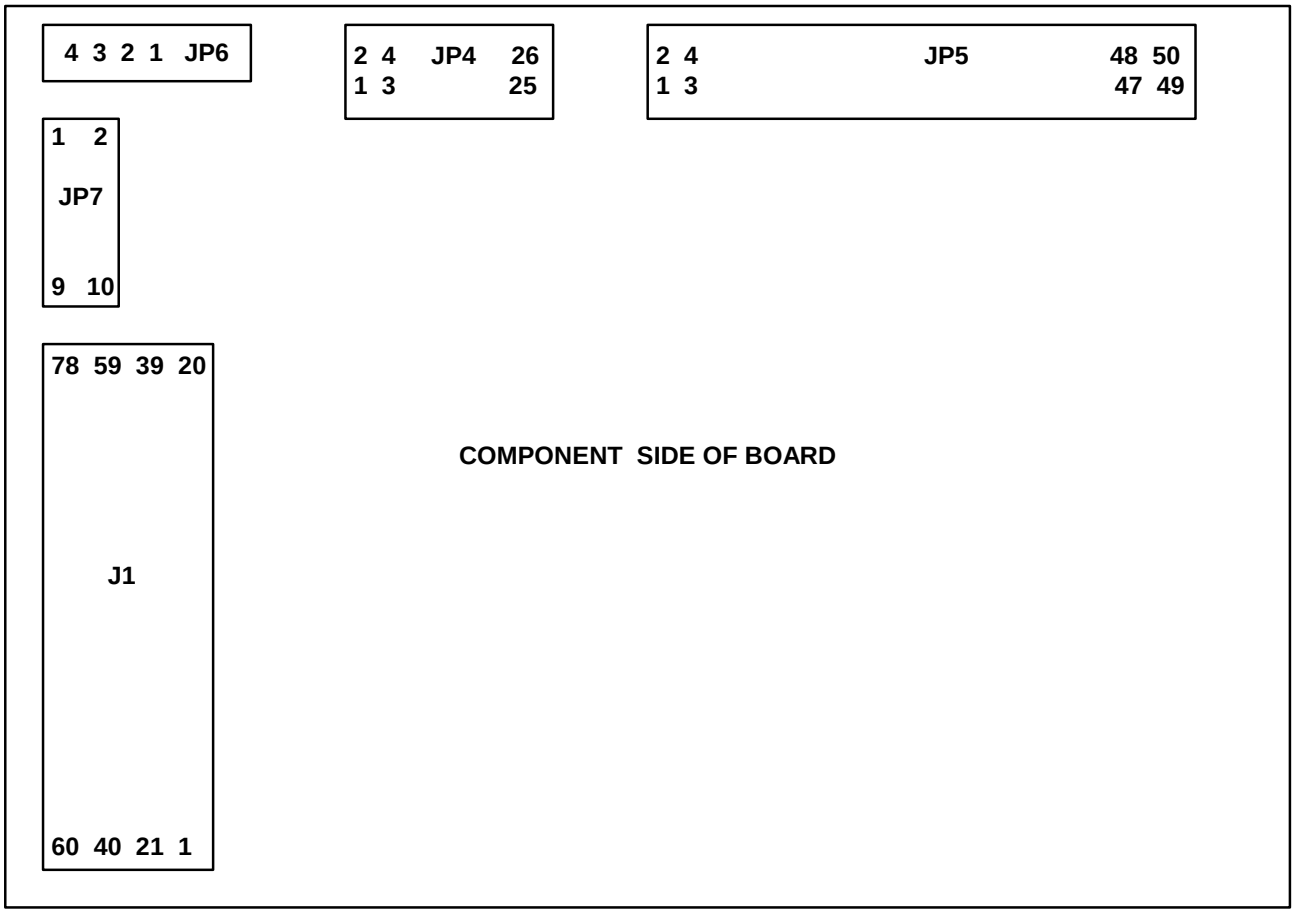


Figure 1

Connector: JP6 Samtec TSW 104-14-L-S
Mate: Amp 87499-4, Keying Plug 86286-1

Pin	Function
1	External Ground
2	External (-12VDC)
3	Removed for Keying
4	External(+12VDC)

TABLE 4

Connector: J1 –8 S/D Channels with up to 4 D/S Channels AMP 748483-5 Mate: AMP 748368-1

Pin	Ch.1 S/D	Pin	Ch.2 S/D	Pin	Ch.3 S/D	Pin	Ch.4 S/D	Pin	Ch.5 S/D	Pin	Ch.6 S/D		
39	S1	18	S1	36	S1	15	S1	33	S1	12	S1		
58	S2	76	S2	55	S2	73	S2	52	S2	70	S2		
78	S3	57	S3	75	S3	54	S3	72	S3	51	S3		
19	S4	37	S4	16	S4	34	S4	13	S4	31	S4		
38	RHi	17	RHi	35	RHi	14	RHi	32	RHi	11	RHi		
77	RLo	56	RLo	74	RLo	53	RLo	71	RLo	50	RLo		
Pin	Ch.7 S/D	Pin	Ch.8 S/D	Pin	Ch.1 D/S	Pin	Ch.2 D/S	Pin	Ch.3 D/S	Pin	Ch.4 D/S	Pin	
30	S1	9	S1	27	S1	6	S1	24	S1	3	S1		
49	S2	67	S2	46	S2	64	S2	43	S2	61	S2		
69	S3	48	S3	66	S3	45	S3	63	S3	42	S3	1 & 40	CHASSIS
10	S4	28	S4	7	S4	25	S4	4	S4	22	S4	21	Int. Exc. Out Hi
29	RHi	8	RHi	26	RHi	5	RHi	23	RHi	2	RHi	60	Int. Exc. Out Lo
68	RLo	47	RLo	65	RLo	44	RLo	62	RLo	41	RLo		

TABLE 5

Connector: J1 –6 D/S Channels with up to 4 S/D Channels

Pin	Ch.1 S/D	Pin	Ch.2 S/D	Pin	Ch.3 S/D	Pin	Ch.4 S/D	Pin		Pin			
39	S1	18	S1	36	S1	15	S1	33	Not used	12	Not used		
58	S2	76	S2	55	S2	73	S2	52	Not used	70	Not used		
78	S3	57	S3	75	S3	54	S3	72	Not used	51	Not used		
19	S4	37	S4	16	S4	34	S4	13	Not used	31	Not used		
38	RHi	17	RHi	35	RHi	14	RHi	32	Not used	11	Not used		
77	RLo	56	RLo	74	RLo	53	RLo	71	Not used	50	Not used		
Pin	Ch.5 D/S	Pin	Ch.6 D/S	Pin	Ch.1 D/S	Pin	Ch.2 D/S	Pin	Ch.3 D/S	Pin	Ch.4 D/S	Pin	
30	S1	9	S1	27	S1	6	S1	24	S1	3	S1		
49	S2	67	S2	46	S2	64	S2	43	S2	61	S2		
69	S3	48	S3	66	S3	45	S3	63	S3	42	S3	1 & 40	CHASSIS
10	S4	28	S4	7	S4	25	S4	4	S4	22	S4	21	Int. Exc. Out Hi
29	RHi	8	RHi	26	RHi	5	RHi	23	RHi	2	RHi	60	Int. Exc. Out Lo
68	RLo	47	RLo	65	RLo	44	RLo	62	RLo	41	RLo		

TABLE 6

Connector: JP4 – For 8 S/D Channels with up to 6 D/S channels.

Amp 103311-6

Auxiliary Slot DB25S Connector / Cable assembly (P/N 07-0010) is supplied with above configuration. Header connector mates with JP4 on board. Signals are routed to 25 pin connector. (Table 7A)

JP4

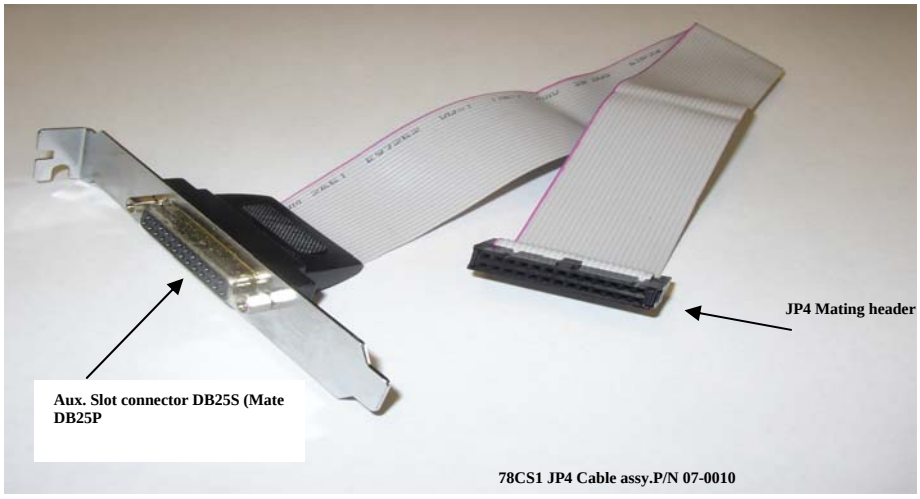
Pin	Ch.5 D/S	Pin	Ch.6 D/S
1	S1	7	S1
3	S2	9	S2
2	S3	8	S3
4	S4	10	S4
5	RHi	11	RHi
6	RLo	12	RLo

TABLE 7

DB25S Mate: DB25P

Pin	Ch.5 D/S	Pin	Ch.6 D/S
1	S1	4	S1
2	S2	5	S2
14	S3	17	S3
15	S4	18	S4
3	RHi	6	RHi
16	RLo	19	RLo

TABLE 7A



Note: S4 pins used only with Resolvers. Do not connect to any undesignated pins.

All S/D and D/S Rhi and RLo reference signals are configured as "***Individual Reference Signals***" and are brought out to the connecter. To configure common references and other combinations, connections must be made externally.

CAUTION: The reference & Signal pins on the male mating connectors for J1 and aux. slot connector DB25P, will have **high voltages** applied to them when power is on. Be certain that power is turned off **before** removing the connector.

NAI convention for synchro/resolver signals is
S3 = + sin S1= - sin S2 = + cos S4 = - cos
When used with external transformers,
S3 = GND S1= - sin S2 = GND S4 = - cos
When used with external SBA amplifier,
S3 = -sin S1= GND S2 = -cos S4 = GND

Quick Reference Guide				
S/D CHANNELS	D/S CHANNELS	78 PIN CONNECTOR	78 Pin w/25 Pin D CONNECTOR	Table Reference
0	2	X		5
0	4	X		5
0	6	X		6
2	2	X		5
2	4	X		5
2	6	X		6
4	2	X		5
4	4	X		5
4	6	X		6
8	2	X		5
8	4	X		5
8	6		X	5 & 7A

TABLE 8

Connector : JP5 Samtec TSW-125-25-T-D-RA

Encoder/Commutation Outputs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	A Hi Ch1	15	B Hi Ch3	31	IDX Hi Ch5	45	A Hi Ch8
2	A Lo Ch1	16	B Lo Ch3	32	IDX Lo Ch5	46	A Lo Ch8
3	B Hi Ch1	17	IDX Hi Ch3	33	A Hi Ch6	47	B Hi Ch8
4	B Lo Ch1	18	IDX Lo Ch3	34	A Lo Ch6	48	B Lo Ch8
5	IDX Hi Ch1	19	A Hi Ch4	35	B Hi Ch6	49	IDX Hi Ch8
6	IDX Lo Ch1	20	A Lo Ch4	36	B Lo Ch6	50	IDX Lo Ch8
7	A Hi Ch2	21	B Hi Ch4	37	IDX Hi Ch6		
8	A Lo Ch2	22	B Lo Ch4	38	IDX Lo Ch6	25	GROUND
9	B Hi Ch2	23	IDX Hi Ch4	39	A Hi Ch7	26	GROUND
10	B Lo Ch2	24	IDX Lo Ch4	40	A Lo Ch7		
11	IDX Hi Ch2	27	A Hi Ch5	41	B Hi Ch7		
12	IDX Lo Ch2	28	A Lo Ch5	42	B Lo Ch7		
13	A Hi Ch3	29	B Hi Ch5	43	IDX Hi Ch7		
14	A Lo Ch3	30	B Lo Ch5	44	IDX Lo Ch7		

TABLE 9

Note: Commutation outputs are differential outputs and are translated as follows:
A = Ch1 A HI & LO; B = Ch1 B HI & LO; C = Ch1 IDX HI & LO

INPUT/OUTPUT CODE TABLE

Code	Input (VL-L)	Ref Vrms	Freq. (Hz)	Tracking rate (rps) at 16 bit		Output (VL-L)	Ref (Vrms)	Freq. (Hz)	Load	Comments
00	No Modules (Reference Module only)									
01	11.8	26	400	150		11.8	26	400	1.2 VA	
02	90	115	400	150		90	115	400	1.2 VA	
03	90	115	50/400	18.5		90	115	400	1.2 VA	
08	2-28	2-28	400	150		26	26	400	1.2 VA	Resolver output only
09	2-28	2-28	400	150		26	26	400	0.13 VA	Synchro output only (5ma output)
10	2-28	2-28	400	150		11.8	26	400	1.2 VA	Synchro or Resolver

TABLE 10

See code list addendum for descriptions of code 11 and above.

PART NUMBER DESIGNATION

76CS1 - XX X X X X - XX

TOTAL NUMBER OF S/D CHANNELS
- 00 = 0 S/D Channels
- 02 = 2 S/D Channels
- 04 = 4 S/D Channels
- 08 = 8 S/D Channels

TOTAL NUMBER OF D/S CHANNELS
- 0 = 0 D/S Channels
- 2 = 2 D/S Channels
- 4 = 4 D/S Channels
- 6 = 6 D/S Channels (1) (2)

ENVIRONMENTAL
- C = 0°C to +70°C
- E = -40°C to +85°C
- H = E With Removable Conformal Coating
- K = C With Removable Conformal Coating

FORMAT
- S = Synchro
- R = Resolver
- M = Mixed (See Code Table)
- P = Programmable Synchro/Resolver (3)

CODE (See Code Table)

ENCODER/COMMUTATION
- - = Without Encoder/Commutation option
- E = With Encoder/Commutation option

OPTIONAL REFERENCE SELECTION
- 0 = No "On Board Reference"
- A = 2-28 VRMS output
- C = 115 VRMS fixed output

(1) Maximum Channel density is fixed at 8 S/D and 6 D/S, which requires using the JP4 connector. See JP4 connector information (Table 7 & 7A).

(2) Selecting 6 channels of D/S with 0, 2 or 4 channels of S/D **only** will be configured to all channels residing on J1 connector. (See Table 6)

(3) Programmable Synchro/Resolver and Encoder/Commutation Options are for Measurement Channels only. If Simulation outputs are also required, code number must be assigned by factory to define output channels.

FOR OTHER VARIATIONS ON TOTAL CHANNEL COUNTS
(S/D AND D/S CONFIGURATIONS), PLEASE CONTACT FACTORY

Revision Page

Revision	Description of Change	Engineer	Date
Rev 2.2	Added header and footer; Corrected specifications for measurement, stimulus & general; Revised descriptions of the S/D & D/S sections; Assigned numbering scheme to tables;Added tables for 12 channel only configuration; Added table for 25 pin D-connector; Added quick reference guide for available combinations; Added 20 digit part number for this model.	WG/BC	10/02/01
Rev 2.3	Added reference options for on and off board reference and option for all D/S ref signals to be available at connector in part number. Corrected Code Table item 58.	WG/BC	10/05/01
Rev 2.4	Corrected font size in S/D description section. Modified description on pg 12 which makes reference to “Common References”.	BC	10/10/01
Rev 2.5	Changing part number back to 15 characters and removing reference options. Updating verbage on pg. 12 which makes reference to “common references”; changing to Individual references. Incorporated 24 bit resolution for 2 speed mode, pg 8.	FH/WG	10/17/01
Rev 2.6	Modified title description page; Added column in revision sheet for engineer.	BC	10/23/01
Rev 2.7	Removed all references made to 12 SD channel configuration; Added 2 speed connectivity description; cleaned up right margins, renumbered tables and notes; Added PCI programming section; Added explanation on 24-bit resolution for two-speed mode. Corrected ‘E’ temperature for range in specification and part number; Deleted “erroneous”; Deleted 2CH S/D option. Corrected general grammer and details. Made corrections to the code table. Added register bit map for Angle Change Register.	FH/BC	12/03/01
Rev 2.8	Added register bit map for Angle Change Register.	BC	12/06/01
Rev 2.9	Added code 59 & 61	FH	12/06/01
Rev 3.0	Added code 65; Register Map D/S Ch.N Data is read/write; Write 0 to Latch Register to disengage latch on all channels.	GS	12/20/01
Rev 3.1	See code list addendum for descriptions of code 50 and above. Added PN 02 for SD Automatically supports either 5V or 3.3V logic levels. Changed S/D read 1-2spd text	GS	02/05/02
3.3	Replaced 150 with 152.5878 rps. Affects Velocity Scale Factor and Vel Output Descriptions	GS	6/27/02
3.4	For proper Soft Reset operation, 1µ < pulsewidth <=50ms.	GS	6/27/02
3.5	Removed 2-13.5 volt reference option (from spec, and PN)	GS	6/28/02
3.6	Clarified Tables 7 and 7A for DS use only.	GS	7/26/02
3.7	Removed JP6-3 for Keying.	GS	8/12/02
3.8	Added Encoder Output & Commutation to SPECIFICATIONS	GS	8/28/02
3.9	EXTERNAL +/- 12VDC: (JP6 & JP7)	GS	10/10/2
3.10	Corrected - = Without Encoder/Commutation option	GS	10/18/02
4.0	Corrected DB25S Mate, pin numbers, Table 7A	GS	11/1/2
4.1	Added code 00 for NO MOUDLES (REFERENCE MODULE ONLY)	GS	12/9/2
4.2	Added D3/POST Simulation test description to page 2. Revealed revision control sheet.	GS	2/4/3
4.3	Two-Speed Read: read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word.	GS	8/6/3
4.4	Added Code 09	GS	9/3/3
4.5	Corrects Code 08 (26 Vrms & 16VL-L) and 09 (0.13VA or 5ma)	GS	11/3/3
4.6	Adds Code 10	GS	12/1/3
4.7	Eliminates Format for Code Table	GS	10/8/4
4.8	JP6 Mate is 87499-7 (not 87499-4)	GS	11/11/4
4.9	UNDER MEMORY MAP, to read Two-Speed data user must first be read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word. Now the same as in description.	GS	3/7/5
5.0	NAI convention for synchro/resolver signals is S3=+sin S1=-sin S2=+cos S4=-cos	GS	5/5/5
5.1	Removed 5 mA output from comments referring to P/N code 10	AS	17 Feb 2006
5.2	Added Aux. cable assy. Picture, reformatted pin out tables, added notes to code table re: codes 8, 9 &10. Added to note 3 for programmable feature. Corrected caution note re: high voltages on mating connectors. Changed address to 110.	FR	1/23/07