Eight (8) LVDT/RVDT Measurement Channels

Eight (8) 2-Wire or 3/4-Wire to Digital Converters, and

Six (6) LVDT/RVDT Stimulus Channels

Six (6) 3/4-Wire or Twelve (12) 2-Wire, Programmable
16 BIT RESOLUTION; WRAP-AROUND SELF TEST
Optional Excitation Supply
Commercial & Military Versions Available

FEATURES:

- 16 Bit Resolution
- Continuous background BIT testing with Excitation and Signal loss detection
- Automatically supports either 5V or 3.3V PCI bus
- Transformer isolated
- 4, 8 and 12 (2 wire) Stimulus channels or
  2, 4 and 6 (3 or 4 wire) Stimulus channels available to
  Mix with 4 or 8 (2, 3, or 4 wire) Measurement channels
- Auto-ranging input between 2.0 and 28 Vrms
- Self-calibrating. Card removal NOT required.
- 360 Hz to 10 kHz operation
- LATCH feature for Measurement
- ON/OFF for Stimulus (D/L) Channels
- Stable output with temperature
- Watchdog timer and soft reset
- No adjustments or trimming required
- Commercial or Extended Temperature
- Part number, S/N, Date code, & Rev. in nonvolatile memory

DESCRIPTION:
This single slot high density intelligent DSP-based card offers up to eight (8) separate transformer isolated programmable LVDT/RVDT-to-Digital tracking converters and up to twelve (12) two-wire, or six (6) three/four-wire transformer isolated "PROGRAMMABLE" LVDT/RVDT outputs and all with wrap-around self-test and optional excitation supply. Instead of buying cards that are set for specific outputs or inputs, the uniqueness of this design makes it possible to buy our combination measurement and stimulus channels whose outputs can be programmed and reprogrammed in the field for any excitation and signal voltage between 2.0 and 28 volts and whose measurement inputs can auto range between 2.0 and 28 volts. Operating frequency between 360Hz and 10 kHz can be specified (see Part Number). This card can be configured for either two-wire or three/four-wire LVDTs.

The measurement channels of this card can be used for 4-wire, 3-wire or 2-wire LVDT inputs. For 4-wire or 3-wire configurations the output is computed as A-B/A+B and is expressed as %FS. For 2-wire configurations, the output is computed as A/B (where A is the a-b signal of the LVDT and B is a constant reference signal) and is expressed as %FS This card uses a derived reference ratio-metric design approach that is insensitive to magnitude, temperature, frequency and phase shift effects. The ratio-metric technique assures that the output will change only when the LVDT position changes and will ignore excitation voltage variations. The LATCH feature permits the user to read all channels at the same time. Reading will unlatch that channel. The converters utilize a Type II servo loop processing technique that enables tracking, at full accuracy, up to the specified rate. Intermediate transparent latches, on all data outputs, guarantee that current valid data is always available for any channel without affecting the tracking performance of the converters. No interrupts or waiting time are required.

For each Stimulus channel, one transformer isolated excitation is supplied for each A, B output pair. The transformation ratio (TR), same for each pair of outputs, sets the maximum output voltage with relation to the excitation voltage (TR = Max Output Voltage / Excitation Voltage). Use of a ratio-metric design eliminates errors caused by excitation voltage variations. The outputs are stable with temperature and switching spikes are not noticeable. A watchdog timer is provided to monitor the processor. To simplify logistics, Part number, S/N, Date code, & Rev. are located in nonvolatile memory locations.

Major diagnostics are incorporated to offer substantial improvements to system reliability because the user is alerted (within 5 seconds) to channel malfunctions. This approach reduces bus traffic because the Status registers do not require constant polling. See Programming Instructions for further details.

The D2 test initiates automatic background BIT testing that for measurement, each channel is checked over the programmed signal range to a measuring accuracy 0.1% FS. For stimulus, background BIT testing compares the output of each channel against the commanded input to a test accuracy of 0.2% FS. BIT also monitors each Signal Output and Excitation. A failure triggers an Interrupt (if enabled) and results are available in *Status Registers*. Testing, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 test for measurement starts an initiated BIT Test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and measures multiple voltages to a test accuracy of 0.1%FS. External excitation for measurement channels is not required. The (D3) test for stimulus channels starts a BIT test that generates and tests 20 different positions to a testing accuracy of 0.2% FS. External reference *is* required. CAUTION: (Stimulus channel) Outputs are active during this test. In any case, testing requires no external programming, and can be Initiated or terminated via the bus. Check connected loads for possible interaction. Any failure triggers an interrupt (if enabled) and results can be read from the *Status Registers*.

The D0 test is used to check the card and the PCI interface. All channels are disconnected from the outside world, allowing user to write any number of input positions to the card and then read the data from the interface. The D0 Test only applies to the Measurement channels. External excitation is not required.

Temperature Range: This board is available for "C" or "E" operating temperature ranges (See part number designation). The "C" version operates from 0°C to +70°C and is populated with standard high quality commercial semiconductors. The "E" version, used for severe environmental condition, operates from -40°C to +85°C and is populated with high quality extended temperature semiconductors.

SPECIFICATIONS:	(For each Measurement channel)
Number of channels:	4 or 8. See part number.
Resolution:	16-bit
Accuracy:	0.025% FS
Bandwidth:	40 Hz. BW and tracking rate can easily be customized.
Input format:	2, 3, or 4-wire LVDT or RVDT
Input voltage	Auto-ranging from 2.0 to 28 Vrms. Transformer isolated.
Excitation voltage:	Not required for computation of output but should be connected to allow card to check for excitation loss.
Input Impedance:	40 kΩ min. at 360 Hz
Frequency:	Specify between 360 Hz to 10 kHz, (See Part Number and Code Table)
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and Output up to ±60° (3-wire units ignore phase shift)
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.

SPECIFICATIONS:	(For each Stimulus channel)
Number of channels:	4, 8 or 12 (2-Wire), or 2, 4 or 6 (3/4-Wire). See part number.
Resolution:	16 bits (.001526% FS)
Linearity:	0.1%FS for .2 <= TR <= 2.0 (.05% FS available at a specified frequency and TR)
Output Format:	Configurable for either 3/4-wire or 2-wire transformer isolated. Output voltage will vary directly with excitation.
Load:	With output voltages from 2.0 to 20.0Vrms: 10 kΩ min.

	With output voltages from 20 to 28.0Vrms: 15 kΩ min. Short circuit protected.
Regulation:	2% max.
Excitation:	2.0 to 28 Vrms. Transformer isolated.
Frequency (excitation):	360 Hz to 10kHz, see code table
Phase Shift (input to output):	3° max
Phase shift (A/B):	0.5°.
Excitation (each) Z in:	50 KΩ min.
Signal Logic Level:	Automatically supports either 5V or 3.3V PCI bus
Power:	+5 VDC ±5% at 0.35 A + 1A (3A peak) @ 5VA Load on optional Excitation Supply ±12 VDC ±5% at 0.5 A

EXCITATION:

EXCITATION:	Optional. (See part number).
Voltage:	2.0–28 Vrms or 115 Vrms fixed; resolution 0.1 Vrms; Accuracy ±2%
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 190mA RMS @ 2-26VAC, 45mA RMS @ 115VAC Note: Power is reduced linearly as the Excitation Voltage decreases.

GENERAL SPECIFICATIONS:

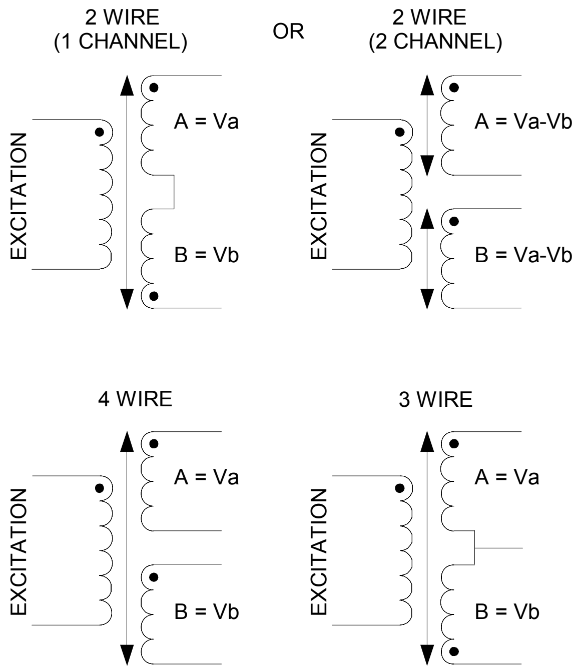
Signal Logic Level:	Automatically supports either 5V or 3.3V PCI bus.	
Power:	See current requirement Table 1 below. Power supplies must be able to supply the peak power without current limiting.	
Temperature, operating:	"C" = 0°C to +70°C, "E" = -40°C to +85°C (See part number)	
Temperature, storage:	-55° C to +105° C	
Size:	3.950 (10.033) height, 12.285 (31.204) length; less front panel connector J1; dimensioned in inches (cm)	
Weight:	Board & heat sink less modules	10 oz. Max.
	L/D modules @ 4 Ch ea.	2.5 oz. Max.
	D/L modules w/ transformers 2Ch ea.	5.0 oz. Max.
	Excitation module	1.8 oz. Max.

CURRENT REQUIREMENTS:

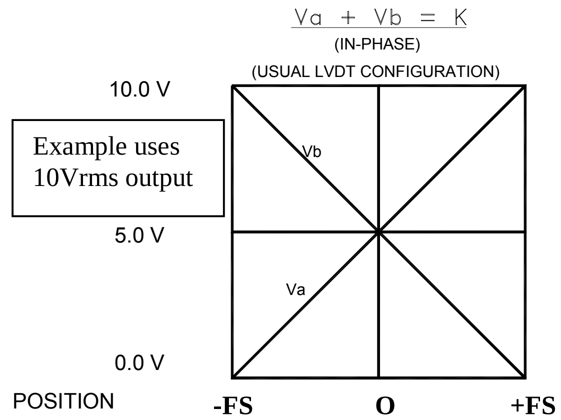
	±12Vdc	**+5Vdc**
Board – no Modules	15mA	460mA
Add per 4 Ch L/D Mod	15mA	160mA
Add per 2 Ch D/L Mod	140mA	35mA
Excitation Module		1A @ 5VA Load (3A Peak)

TABLE 1

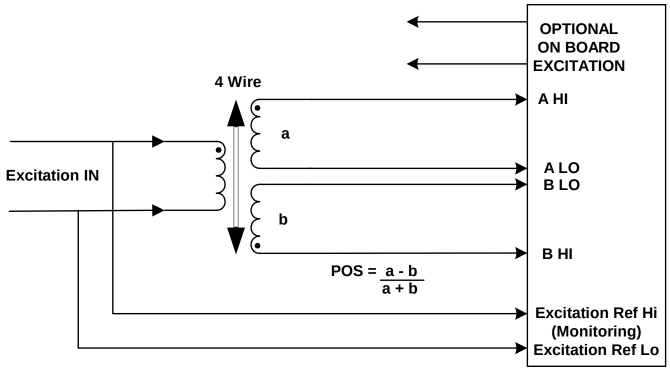
Principal of Operation (LVDT): Typically the primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

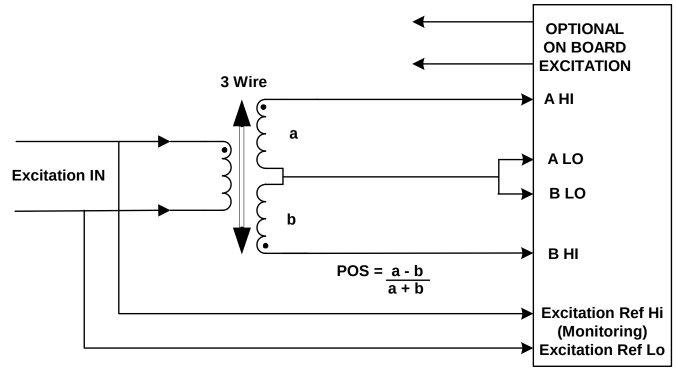


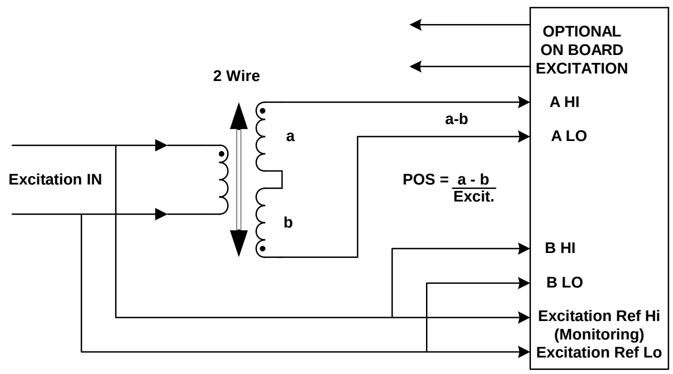
POSITION = (Va-Vb) / (Va+Vb)



Va+Vb=10V	Va+Vb=10V	Va+Vb=10V
Va-Vb=10V	Va-Vb=0V	Va-Vb=10V
Va=0V	Va=5V	Va=10V
Vb=10V	Vb=5V	Vb=0V







Interfacing the LVDT to the Converter for Measurement: Two common connection methods are:

1. Primary as reference (two-wire system) This method of connection converts the widest range of LVDT sensors and is the most sensitive to excitation voltage variations, temperature and phase shift effects.

2. Derived reference (three/four-wire LVDT) The LVDT is again excited from the primary side, but the converter reference is the sum of A + B that has constant amplitude for changing core displacement. This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity (A-B)/(A+B)

Configuring Stimulus Channels for 2 and 3/4-Wire Outputs: When referring to the register map make note that there are references made to channels 1A & B through 4A & B. For channels programmed for 3/4-wire mode, the A&B Position Data Registers are shared. Therefore, only Position Data Register A is set when configuring the registers. The card can be programmed for use in combination, but as previously stated, the 3/4-wire channels are paired off with the same number channel A & B and cannot be separated.

Channels programmed for 2-wire mode, the A & B outputs are set individually allowing for up to a total of 8 separate output channels. I.e., the output Ch1 A will produce a voltage equivalent to the Va-Vb voltage of a 2 wire system representing the Position in Ch 1 A Data Register, and Ch1 B will produce the equivalent voltage representing the Position in Ch1 B Data Register.

PROGRAMMING INSTRUCTIONS:

MEMORY MAP

000	L/D Ch.1 Data	read	0A0	(A&B) resolution Ch. 8	read/write	140	Wrap-around D/L Ch.3B	read
004	L/D Ch.2 Data	read	0A4	Velocity Scale Ch. 1	read/write	144	Wrap-around D/L Ch.4A	read
008	L/D Ch.3 Data	read	0A8	Velocity Scale Ch. 2	read/write	148	Wrap-around D/L Ch.4B	read
00C	L/D Ch.4 Data	read	0AC	Velocity Scale Ch. 3	read/write	14C	Wrap-around D/L Ch.5A	read
010	L/D Ch.5 Data	read	0B0	Velocity Scale Ch. 4	read/write	150	Wrap-around D/L Ch.5B	read
014	L/D Ch.6 Data	read	0B4	Velocity Scale Ch. 5	read/write	154	Wrap-around D/L Ch.6A	read
018	L/D Ch.7 Data	read	0B8	Velocity Scale Ch. 6	read/write	158	Wrap-around D/L Ch.6B	read
01C	L/D Ch.8 Data	read	0BC	Velocity Scale Ch. 7	read/write	19C	2-3/4 Wire Mode **D/L**	read/write
020	L/D Velocity Ch. 1	read	0C0	Velocity Scale Ch. 8	read/write	1A0	Status, Signal **D/L**	read
024	L/D Velocity Ch. 2	read	0C4	Magnitude (A+B) Ch.1	read/write	1A4	Status,Excitation **D/L**	read
028	L/D Velocity Ch. 3	read	0C8	Magnitude (A+B) Ch.2	read/write	1A8	Status,Test **D/L**	read
02C	L/D Velocity Ch. 4	read	0CC	Magnitude (A+B) Ch.3	read/write	1AC	Active channels **D/L**	read/write
030	L/D Velocity Ch. 5	read	0D0	Magnitude (A+B) Ch.4	read/write	1B0	Test (D2) verify **D/L**	read/write
034	L/D Velocity Ch. 6	read	0D4	Magnitude (A+B) Ch.5	read/write	1B4	Test Enable **D/L**	read/write
038	L/D Velocity Ch. 7	read	0D8	Magnitude (A+B) Ch.6	read/write	1B8	Outputs ON/OFF	read/write
03C	L/D Velocity Ch. 8	read	0DC	Magnitude (A+B) Ch.7	read/write	1BC	Interrupt Enable	read
040	Scale Ch.1	read/write	0E0	Magnitude (A+B) Ch.8	read/write	1C0	Interrupt Status	read/write
044	Scale Ch.2	read/write	0E4	Position Ch. 1A Data	read/write	1C4	Frequency (Exc. Supply)	read/write
048	Scale Ch.3	read/write	0E8	Position Ch. 1B Data (2-wire)	read/write	1C8	Voltage (Exc. Supply)	read/write
04C	Scale Ch.4	read/write	0EC	Position Ch. 2A Data	read/write	1CC	Watchdog timer	read/write
050	Scale Ch.5	read/write	0F0	Position Ch. 2B Data (2-wire)	read/write	1D0	Soft reset	write
054	Scale Ch.6	read/write	0F4	Position Ch. 3A Data	read/write	1D4	Part #	read
058	Scale Ch.7	read/write	0F8	Position Ch. 3B Data (2-wire)	read/write	1D8	Serial #	read
05C	Scale Ch.8	read/write	0FC	Position Ch. 4A Data	read/write	1DC	Date code	read
060	Active channels **L/D**	read/write	100	Position Ch. 4B Data (2-wire)	read/write	1E0	Rev level PCB	read
064	Test (D2) verify **L/D**	read/write	104	Position Ch. 5A Data	read/write	1E4	Rev level DSP Master	read
068	Test Enable **L/D**	read/write	108	Position Ch. 5B Data (2-wire)	read/write	1E8	Rev level FPGA Master	read
06C	Status, Signal **L/D**	read	10C	Position Ch. 6A Data	read/write	1EC	Rev level DSP Slave	read
070	Status,Excitation **L/D**	read	110	Position Ch. 6B Data (2-wire)	read/write	1F0	Rev level FPGA Slave	read
074	Status,Test **L/D**	read	114	Transformer Ratio Ch. 1	read/write	1F4	Rev level Interface FPGA	read
078	Latch	write	118	Transformer Ratio Ch. 2	read/write	1F8	Board Ready	read
07C	LVDT/D Test Position	read/write	11C	Transformer Ratio Ch. 3	read/write			
080	2-3/4 Wire Mode	read/write	120	Transformer Ratio Ch. 4	read/write			
084	(A&B) resolution Ch. 1	read/write	124	Transformer Ratio Ch. 5	read/write			
088	(A&B) resolution Ch. 2	read/write	128	Transformer Ratio Ch. 6	read/write			
08C	(A&B) resolution Ch. 3	read/write	12C	Wrap-around D/L Ch.1A	read			
090	(A&B) resolution Ch. 4	read/write	130	Wrap-around D/L Ch.1B	read			
094	(A&B) resolution Ch. 5	read/write	134	Wrap-around D/L Ch.2A	read			
098	(A&B) resolution Ch. 6	read/write	138	Wrap-around D/L Ch.2B	read			
09C	(A&B) resolution Ch. 7	read/write	13C	Wrap-around D/L Ch.3A	read			

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Latch Outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Test Enable **L/D**	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Active channels **L/D**	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test **L/D**	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Signal **L/D**	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Excitation **L/D**	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
2 or 3,4 wire Input **L/D**	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Test Enable **D/L**	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Active channels **D/L**	X	X	X	X	Ch.6B	Ch.6A	Ch.5B	Ch.5A	Ch.4B	Ch.4A	Ch.3B	Ch.3A	Ch.2B	Ch.2A	Ch.1B	Ch.1A
Outputs ON/OFF	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test **D/L**	X	X	X	X	Ch.6B	Ch.6A	Ch.5B	Ch.5A	Ch.4B	Ch.4A	Ch.3B	Ch.3A	Ch.2B	Ch.2A	Ch.1B	Ch.1A
Status, Signal **D/L**[2]	X	X	X	X	X	Ch.6A	X	Ch.5A	X	Ch.4A	X	Ch.3A	X	Ch.2A	X	Ch.1A
Status, Excitation **D/L**	X	X	X	X	X	Ch.6A	X	Ch.5A	X	Ch.4A	X	Ch.3A	X	Ch.2A	X	Ch.1A
2 or 3,4 wire Output **D/L**[3]	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Enable/Status	X	X	X	X	X	#6	#5	#4	X	X	X	X	#3	X	#2	#1
(A&B) resolution	D15	X	X	X	X	X	X	X	X	X	X	X	X	**D2**	**D1**	**D0**

↑ "0"= Encoder
"1"= Commutation

TABLE 3

	D2	D1	D0
16 bit	0	0	0
15 bit	0	0	1
14 bit	0	1	0
13 bit	0	1	1
12 bit	1	0	0

Encoder Outputs ↑

Note 1 - Values are rounded off
Note 2 - '0' = 3 or 4 wire; '1' = 2 wire
Note 3 - Signal status is not monitor for 2-wire

INTERRUPT ENABLE & STATUS REGISTERS:

#1 = L/D Signal Loss
#2 = L/D Excitation Loss
#3 = L/D Test Accuracy Error
#4 = D/L Signal Loss
#5 = D/L Excitation Loss
#6 = D/L Test Accuracy Error

Measurement (L/D) Specific Registers

Active Channels, L/D: Set the bit, corresponding to each channel to be monitored during BIT testing, in the *L/D Active Channel Register*. "1"=active; "0"=not used. Omitting this step will produce false alarms because unused channels will set faults.

Selecting 2 or 3,4 Wire operation: Program the corresponding bit for the appropriate channel in the *2-3/4 Wire Register*. Logic '1' = 2 wire; Logic '0' = 3 or 4 wire.

Data Format:

For 4-wire or 3-wire inputs, the output data is A-B/A+B and represents %FS. Format is two's complement. Maximum positive excursion is 32767 (7FFFh), 0 = 0, and maximum negative excursion is -32768 (8000h).

For 2-wire input, the output data is A-B/Excitation and represents %FS. Format is two's complement. Maximum positive excursion is 32767 (7FFFh), 0 = 0, and maximum negative excursion is -32768 (8000h).

Programming Scale Registers

The 4-wire or 3-wire LVDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs, no scaling is required because the inputs are auto-ranging, however the corresponding *Scale Register* can be used to scale the output code.

Default settings for the *Scale Registers* are set to 65535 (FFFFh) which results in a full-scale output reading for full travel of the LVDT. A full-scale output reading for less than full travel of the LVDT can be obtained by writing a scale value to the corresponding *Scale Register*. For example, writing 32768 (8000h) to *Scale Ch. 1 Register* will result in channel 1 having a full-scale output reading for one-half travel of the LVDT.

For 2-wire input, the default settings for the *Scale Registers* are 65535 (FFFFh), which result in a full-scale output reading for full travel of the LVDT for TR = 1 (transformation ratio). To achieve full output readings for TR < 1, a scale factor (SF) should be programmed into the corresponding *Scale Register*. This is calculated from the equation:
SF =65535 (FFFFh) x TR

The calculated SF value is written to the corresponding *Scale Register.*

Read (A+B): Read binary number from the *(A+B) Magnitude Register* and multiply by 0.01 Volt. Only valid for 3 or 4 wire configurations.

Velocity Scale Factor: The velocity scale factor is used to achieve a greater resolution at lower translation speeds (Strokes per second, or SPS). The scale factor is: **4095(152.5878SPS/max SPS),** where the max SPS is selected by the user to achieve the maximum resolution for a desired SPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 SPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 SPS for CW rotation, and –32,768 (8000h) being 152.5878 SPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 SPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh; (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h (lowest setting)

Velocity Output: Read Velocity registers of each channel as a 2's complement word, with 7FFFh being max. CW rotation, and 8000h being max. CCW rotation.

When max. velocity is set to 152.5878 SPS, an actual speed of 10 SPS would be read as 0863h.
When max. velocity is set to 152.5878 SPS, an actual speed of -10 SPS would be read as F79Ch.
When max. velocity is set to 50.8626 SPS, an actual speed of 10 SPS would be read as 192Ah.
When max. velocity is set to 50.8626 SPS, an actual speed of -10 SPS would be read as E6D5h.

To convert a velocity word to SPS: **Velocity in SPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 SPS, then
Velocity in SPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 SPS

Latch: All channels may be latched by writing a "2" to D1 in the *Latch Register*. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

Test Enable (D2): Writing "1" to D2 of the *L/D Test Enable Register* initiates automatic background BIT testing. For Measurement, each channel is checked over the programmed Signal range to a measuring accuracy 0.1%FS. A "0" deactivates this test. This test is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The card will write 55h to the associated *L/D Test D2 Verify Register* when D2 Test is enabled. User can periodically clear to 00h and then read the *Test D2 Verify Register* again, after 30 seconds, to verify that background BIT testing is activated.

In addition, each Excitation input and Signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the associated *L/D Signal* and *L/D Excitation Status Registers*

D3 Test Enable: Writing a "1" to D3 in the *L/D Test Enable Register*, starts an off-line BIT test. For Measurement, D3 disconnects all channels from the outside world and connects them across an internal stimulus that generates multiple test voltages that are measured to a test accuracy of 0.1%FS. Test cycle takes about 10 seconds and results can be read from the Test Status Register when D3 changes from "1" to "0". External excitation is not required. An Interrupt, if enabled, will be generated if a BIT failure is detected (See *Interrupt Register*). Testing requires no external programming and can be terminated by writing "0" to D3 of the *Test Enable Register*.

Signal and Excitation monitoring is disabled during D3 test.

D0 Test Enable: Checks the card and interface. Writing a "1" to D0 in the *Test Enable Register* disconnects all channels from the outside world, allowing user to write any number of input positions to the card in the *LVDT/D Test Position Register* and then reads the data from the PCI bus (allow 50 ms before reading). External excitation is not required.

Signal and Excitation monitoring is disabled during D0 test.

Status, Test: Check the corresponding bit of the *L/D Test Status Register*, for status of BIT testing for each active channel. A "1" =Accuracy OK; "0" = failed. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the Test Status Register. Reading will unlatch register.

Status, Excitation: Check the channel's corresponding bit of the *L/D Excitation Status Register*, for status of the Excitation input for each active channel. A "1" = Excitation. ON, "0" = Excitation. loss. Channels that are inactive are also set to "0". (Excitation loss is detected after 2 seconds). Excitation monitoring is disabled during D3 or D0 Test. Any Excitation status failure, transient or intermittent will latch the Excitation *L/D Status Register*. Reading will unlatch register.

Status, Signal: Check the channel's corresponding bit of the *L/D Signal Status Register*, for status of the input signals for each active channel. A "1" = Signal ON, "0" = Signal loss. Channels that are inactive are also set to "0".

(Signal loss is detected after 2 seconds). Any Signal status failure, transient or intermittent will latch the *L/D Signal Status Register*. Reading will unlatch register.

Optional (A&B) Encoder Resolution: To set Encoder Mode, write a "0" to the D15 bit and the appropriate code for the desired resolution to the D2, D1 & D0 bits of the corresponding channel (*A&B) Resolution/Poles Register*. Changing the resolution for any channel can be done on the fly. The default is a 12bit resolution encoder output. See Table 3. **Note**: Encoder/Commutation outputs are optional; see part ordering information.

Stimulus (D/L) Specific Registers

Active Channels, D/L: Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel Register* ("1"=active; "0"=not used). **Omitting this step will produce erroneous errors on unused channels causing false alarms**; hence unused channels will set faults, i.e. status bits, interrupts, etc.

Note: Signal and Excitation status is not monitored in 2-wire mode.

Outputs ON/OFF: Set the bit corresponding to each stimulus channel to be turned on, to "1" in the *Output On/Off Register*. To turn OFF a channel, set corresponding bit to "0". Both channels A & B are controlled simultaneously. i.e. in 2-wire mode the A & B channel pairs are controlled concurrently. Default: Set to OFF.

2-Wire or 3/4-Wire Mode: Set the bit corresponding for each output channel pair (A & B) in the *2-3/4 Wire Mode Register*. Setting the bit to "0" => 3/4 wire mode; Setting the bit to "1" => 2 wire mode. When setting a channel pair to 2-wire mode both channels, A & B of that number pair will be set for 2-wire. Factory default is 3/4-wire mode.

Position Output: Enter the position as a 2's complement number in the corresponding *Position Ch. Data Register* within the range of -1.00 < Position < (+1.00 – lsb). In 3/4-wire mode, position is written only to the A channel of that number pair. The B channel register is ignored. In 2-wire mode the A and B channels are set independently. Factory default: POSITION = 0

Calculate using: register value = POSITION * 32768

Example: For a POSITION = -0.5 -> register value = -0.5 * 32768 = -16384 (0xC000)
Example: For a POSITION = 0.75 -> register value = 0.75 * 32768 = 24576 (0x6000)

The Output voltages in 3/4-wire mode are related to the position by:
Va = Excitation Voltage * TR * (0.5 * Position + 0.5)
Vb = Excitation Voltage * TR * (1 - (0.5 * Position + 0.5))

The Output voltage in 2-wire mode is related to the position by:
V = Excitation Input * TR * Position

Transformation Ratio (TR): Enter the transformation ratio as an integer for each channel pair (A & B) in the *Transformation Ratio Channel Register*. When entering a ratio for channels that are configured for 2-wire mode, both channels A & B of that number pair will have the same transformation ratio. Factory default TR = 1.
Set the TR using the following formula:

TR register value = TR * 1000

Example: For a TR of 0.5 -> TR register value = 0.5 * 1000 = 500 (01F4h)
The valid range of TR is: $0.00 \leq TR \leq 2.00$.

NOTE: TR * Input Voltage must be less than 28V

Test Enable (D2): Writing "1" to D2 of the *D/L Test Enable Register* initiates automatic background BIT testing. For Stimulus, BIT compares the output of each channel with the commanded input to a testing accuracy of 0.2%FS. Outputs must be ON and Excitation supplied for test to function. A "0" deactivates this test. This test is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The card will write 55h to the associated *D/L Test D2 Verify Register* when D2 Test is enabled. User can periodically clear to 00h and then read the *D/L Test D2 Verify Register* again, after 30 seconds, to verify that background BIT testing is activated.

In addition, each Excitation input and Signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the associated *D/L Signal* and *D/L Excitation Status Registers*. Note: Signal Monitoring for Stimulus Channels is not valid in 2-wire mode.

Test Enable (D3): Writing "1" to D3 of the *D/L Test Enable Register* initiates a BIT test that generates and tests 20 different inputs, to a testing accuracy of 0.2%FS. Test cycle takes about 45 seconds and results can be read from the Test Status register when D3 bit changes from "1" to "0" and if enabled, an interrupt will be generated if a BIT failure is detected (See *Interrupt Register*). The testing can be terminated at any time by writing "0" to D3 bit of the *Test Enable Register*. Excitation is required. **CAUTION:** During the (D3) test, the outputs are active. Verify that changing those outputs will not effect connected equipment.

Status, Test: Check the corresponding bit of the *D/L Test Status Register* for status of BIT Testing for each active channel. A "1" means Accuracy OK; "0" failed. Channels that are inactive are also set to "0". (Test cycle takes 2 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register.

Status, Excitation: Check the corresponding bit of the *D/L Excitation Status Register* for status of the excitation input for each active channel. A "1" means Excitation ON, "0" means Excitation Loss on active channels. Channels that are inactive are also set to "0". (Excitation loss is detected after 2 seconds). Note: The Excitation voltage is shared among the channel pairs, however each channel pair can have distinct external excitation voltages. *Excitation* monitoring is always enabled. Any *Excitation* status failure, transient or intermittent will latch the *D/L Excitation Status Register*. Reading will unlatch register.

Status, Sig: Signal status is only available in 3 or 4–wire mode**.** Check the corresponding bit of the *D/L Signal Status Register* for status of the output signal for each active channel. A "1" means Signal is valid, "0" means Signal loss. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Signal monitoring is always enabled (except in 2 wire mode). Any Signal status failure, transient or intermittent will latch the *D/L Signal Status Register*. Reading will unlatch register.

Read Wrap-Around Position: Wrap-around positions are read from the *D/L Wrap-around Channel Registers*. Each enabled D/L channel is measured prior to the transformer output and can be read from the corresponding *D/L Wrap-around Channel Register*. The generated result is a 16-bit binary word (or 16-bit 2's compliment word) that represents position. The data is available at any time. **Note:** In 3/4-wire mode, only channels 1-6A need to be read.

General Use Registers

Interrupt Enable Registers: Interrupts can be enabled to report specific problems/failures detected by the card. The problem/failures that generate these interrupts are:

L/D Signal Loss, L/D Excitation Loss, L/D Test Accuracy Error
D/L Signal Loss, D/L Excitation Loss, D/L Test Accuracy Error

Each external interrupt can be enabled individually. This is accomplished by writing a "1" to the bit corresponding interrupts to the *Interrupt Enable Register* and a "0" to disable those interrupts not used. Refer to Table 2.

Interrupt Status Registers: When an interrupt is initiated via a problem/failure, the *Interrupt Status Register* can be interrogated by a read to identify, which interrupt occurred. Refer to the Register Bit Map. Register is latched when interrupt is generated and unlatched when read.

Note: This register is typically read and cleared by the device driver. Subsequent readings of this register will give clear status.

Optional Excitation Output Frequency: Enter the excitation output frequency as an integer, directly in Hz in the *Frequency Register*.

Example: For a Excitation Output Frequency of 1000Hz -> register value = 1000 (03E8h)
The valid range is: $360 \leq$ Freq $\leq$ 10KHz
Factory default is: F = 400Hz
It is recommended that user program the required frequency before setting the output voltage.

Optional Excitation Output Voltage: Enter the output reference voltage as an integer in the *Voltage Register*. Set the Excitation output voltage using the following formula:

Exc. Out voltage register value = V * 10
Example: For a Excitation output voltage of 7V -> register value = 7 * 10 = 70 (0046h)
The valid range is: 0.0 or $2.0 \leq V \leq 28.0$, with 0.1 volt resolution.
Factory default is: V = 0V

Note: Units supplied with high voltage reference supply can only be set to 0.0 or 115 volts.

Soft Reset: Write an integer "1" to *Soft Reset Register*, then clear to 0 before 50ms elapses. **CAUTION: Register is level sensitive and for proper card operation, the logic level "1", or pulsewidth, must be <= 50ms**. Considering minimum and maximum, 1 μs < pulsewidth <= 50ms. Processor reboots in about 400 ms, after which calibration procedures begin. This function is equivalent to a power-on reset.

Watchdog timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 μSec. The inverted code stays in the register until replaced by a new code. The user should interrogate the *Watchdog Timer Register* after 100 μSec for the inverted code to confirm that the processor is operating.

Part Number: Read as a 16 bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: Read as a 16 bit binary word from the *Serial Number Register*.

Date Code: Read as decimal number from the *Date Code Register*.
Four digits represent YYWW (Year, Year, Week, Week)

Rev Levels: There are a total of 4 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Rev level PCB
Rev level DSP
Rev level FPGA
Rev level Interface FPGA

Software - PCI Programming

This section provides programmers the information needed for developing drivers other than those supplied.
The following information resides in the PCI configuration registers:

Device ID	= 7651	(hex)
Vendor ID	= 15AC	(hex)
Rev	= 01	(hex)
Subsystem ID	= 0001	(hex)
Subsystem Vendor ID	= 15AC	(hex)

Base Address = Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information.
Required Address space = 1K for each card.

EXTERNAL +/- 12VDC: (JP6 & JP7)

The card is shipped and configured for operation with +/- 12 VDC power, being supplied from edge connector.

To operate from External +/- 12VDC supplies: On jumper block JP7, remove jumpers 1-2, and 5-6, then re-connect jumpers 3-4 and 7-8. Leave jumper 9 – 10 connected.

Connect external +12 VDC to JP6-4, connect external –12 VDC to JP6-2 and external ground to JP6-1.

Pin JP6-3 has been removed for keying. We recommend customer plug receptacle pin 3 to insure proper connection and avoid damage.

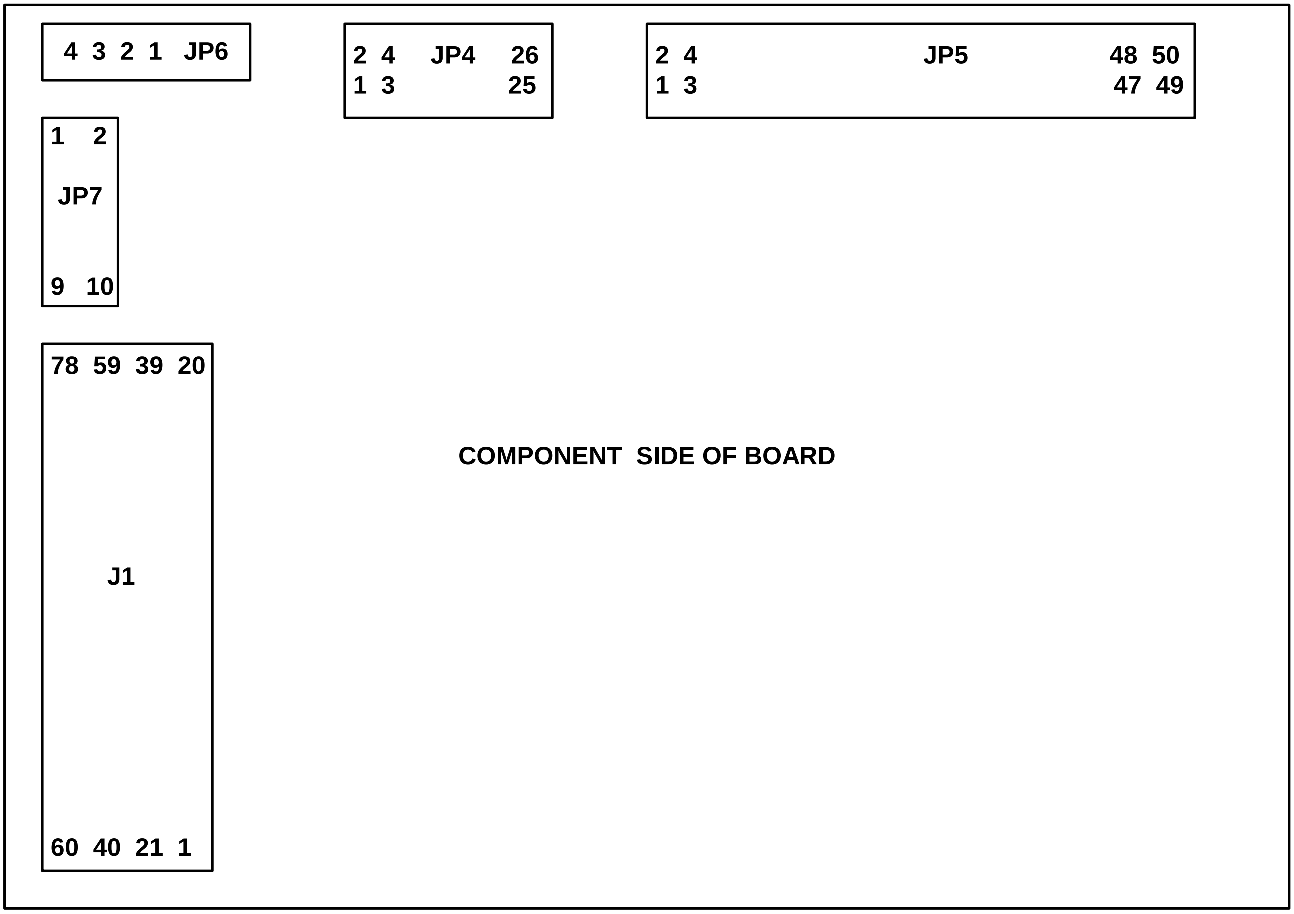


Figure 1

Connector: JP6 Samtec TSW 104-14-L-S
Mate: Amp 87499-4, Keying Plug 86286-1

Pin	Function
1	External Ground
2	External (-12VDC)
3	Removed for Keying
4	External(+12VDC)

TABLE 4

Connector: J1 –8 L/D Channels with up to 4 D/L Channels

AMP 748483-5 Mate: AMP 748368-1

L/D | D/L

Pin	Ch.1 L/D	Pin	Ch.2 L/D	Pin	Ch.3 L/D	Pin	Ch.4 L/D	Pin	Ch.5 L/D	Pin	Ch.6 L/D		
39	A Lo	18	A Lo	36	A Lo	15	A Lo	33	A Lo	12	A Lo		
58	B Hi	76	B Hi	55	B Hi	73	B Hi	52	B Hi	70	B Hi		
78	A Hi	57	A Hi	75	A Hi	54	A Hi	72	A Hi	51	A Hi		
19	B Lo	37	B Lo	16	B Lo	34	B Lo	13	B Lo	31	B Lo		
38	Exc Hi	17	Exc Hi	35	Exc Hi	14	Exc Hi	32	Exc Hi	11	Exc Hi		
77	Exc Lo	56	Exc Lo	74	Exc Lo	53	Exc Lo	71	Exc Lo	50	Exc Lo		
Pin	Ch.7 L/D	Pin	Ch.8 L/D	Pin	Ch.1 D/L	Pin	Ch.2 D/L	Pin	Ch.3 D/L	Pin	Ch.4 D/L	Pin	
30	A Lo	9	A Lo	27	A Lo	6	A Lo	24	A Lo	3	A Lo		
49	B Hi	67	B Hi	46	B Hi	64	B Hi	43	B Hi	61	B Hi		
69	A Hi	48	A Hi	66	A Hi	45	A Hi	63	A Hi	42	A Hi	1 & 40	CHASSIS
10	B Lo	28	B Lo	7	B Lo	25	B Lo	4	B Lo	22	B Lo	21	Int. Exc. Out Hi
29	Exc Hi	8	Exc Hi	26	Exc Hi	5	Exc Hi	23	Exc Hi	2	Exc Hi	60	Int. Exc. Out Lo
68	Exc Lo	47	Exc Lo	65	Exc Lo	44	Exc Lo	62	Exc Lo	41	Exc Lo		

TABLE 5

Connector: J1 –6 D/L Channels with up to 4 L/D Channels

L/D | D/L

Pin	Ch.1 L/D	Pin	Ch.2 L/D	Pin	Ch.3 L/D	Pin	Ch.4 L/D	Pin		Pin			
39	A Lo	18	A Lo	36	A Lo	15	A Lo	33	Not used	12	Not used		
58	B Hi	76	B Hi	55	B Hi	73	B Hi	52	Not used	70	Not used		
78	A Hi	57	A Hi	75	A Hi	54	A Hi	72	Not used	51	Not used		
19	B Lo	37	B Lo	16	B Lo	34	B Lo	13	Not used	31	Not used		
38	Exc Hi	17	Exc Hi	35	Exc Hi	14	Exc Hi	32	Not used	11	Not used		
77	Exc Lo	56	Exc Lo	74	Exc Lo	53	Exc Lo	71	Not used	50	Not used		
Pin	Ch.5 D/L	Pin	Ch.6 D/L	Pin	Ch.1 D/L	Pin	Ch.2 D/L	Pin	Ch.3 D/L	Pin	Ch.4 D/L	Pin	
30	A Lo	9	A Lo	27	A Lo	6	A Lo	24	A Lo	3	A Lo		
49	B Hi	67	B Hi	46	B Hi	64	B Hi	43	B Hi	61	B Hi		
69	A Hi	48	A Hi	66	A Hi	45	A Hi	63	A Hi	42	A Hi	1 & 40	CHASSIS
10	B Lo	28	B Lo	7	B Lo	25	B Lo	4	B Lo	22	B Lo	21	Int. Exc. Out Hi
29	Exc Hi	8	Exc Hi	26	Exc Hi	5	Exc Hi	23	Exc Hi	2	Exc Hi	60	Int. Exc. Out Lo
68	Exc Lo	47	Exc Lo	65	Exc Lo	44	Exc Lo	62	Exc Lo	41	Exc Lo		

TABLE 6

Connector: JP4 – For 8 L/D Channels with up to 6 D/L channels.

Amp 103311-6 **Auxiliary Slot DB25S Connector is supplied with above configuration. Header connector mates with J4P on board. Signals are routed to 25 pin connector. (Table 7A)**

D/L

JP4

Pin	Ch.5 D/L	Pin	Ch.6 D/L
1	A Lo	7	A Lo
3	B Hi	9	B Hi
2	A Hi	8	A Hi
4	B Lo	10	B Lo
5	Exc Hi	11	Exc Hi
6	Exc Lo	12	Exc Lo

TABLE 7

D/L

DB25S Mate: DB25P

Pin	Ch.5 D/L	Pin	Ch.6 D/L
1	A Lo	4	A Lo
2	B Hi	5	B Hi
14	A Hi	17	A Hi
15	B Lo	18	B Lo
3	Exc Hi	6	Exc Hi
16	Exc Lo	19	Exc Lo

TABLE 7A

Note: B Lo pins used only with Resolvers. Do not connect to any undesignated pins.

All L/D and D/L Exc Hi and Exc Lo reference signals are configured as "***Individual Excitation Signals***" and are brought out to the connecter. To configure common references and other combinations, connections must be made externally.

CAUTION: The reference pins on the male mating connector, JP5, will have **high voltages** applied to them when power is on. Be certain that power is turned off **before** removing the connector.

Quick Reference Guide

L/D CHANNELS	D/L CHANNELS	78 PIN CONNECTOR	78 Pin w/25 Pin D CONNECTOR	Table Reference
0	2	X		5
0	4	X		5
0	6	X		6
2	2	X		5
2	4	X		5
2	6	X		6
4	2	X		5
4	4	X		5
4	6	X		6
8	2	X		5
8	4	X		5
8	6		X	5 & 7A

TABLE 8

Connector : JP5 Samtec TSW-125-25-T-D-RA

Encoder/Commutation Outputs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	A Hi Ch1	15	B Hi Ch3	31	IDX Hi Ch5	45	A Hi Ch8
2	A Lo Ch1	16	B Lo Ch3	32	IDX Lo Ch5	46	A Lo Ch8
3	B Hi Ch1	17	IDX Hi Ch3	33	A Hi Ch6	47	B Hi Ch8
4	B Lo Ch1	18	IDX Lo Ch3	34	A Lo Ch6	48	B Lo Ch8
5	IDX Hi Ch1	19	A Hi Ch4	35	B Hi Ch6	49	IDX Hi Ch8
6	IDX Lo Ch1	20	A Lo Ch4	36	B Lo Ch6	50	IDX Lo Ch8
7	A Hi Ch2	21	B Hi Ch4	37	IDX Hi Ch6		
8	A Lo Ch2	22	B Lo Ch4	38	IDX Lo Ch6	25	GROUND
9	B Hi Ch2	23	IDX Hi Ch4	39	A Hi Ch7	26	GROUND
10	B Lo Ch2	24	IDX Lo Ch4	40	A Lo Ch7		
11	IDX Hi Ch2	27	A Hi Ch5	41	B Hi Ch7		
12	IDX Lo Ch2	28	A Lo Ch5	42	B Lo Ch7		
13	A Hi Ch3	29	B Hi Ch5	43	IDX Hi Ch7		
14	A Lo Ch3	30	B Lo Ch5	44	IDX Lo Ch7		

TABLE 9

Note: Commutation outputs are differential outputs and are translated as follows:
A = Ch1 A Hi & Lo; B = Ch1 B Hi & Lo; C = Ch1 IDX Hi & Lo

CODE TABLE

Code	Frequency (Hz)	Notes
01	400	
02	2.8k - 3.2K	
03	2K	
04	2.69K	
05	3K	

See code list addendum for descriptions of code 50 and above.

PART NUMBER DESIGNATION

76CL1 - XX X X L X - XX

TOTAL NUMBER OF L/D CHANNELS
00 = 0 L/D Channels
02 = 2 L/D Channels
04 = 4 L/D Channels
08 = 8 L/D Channels

TOTAL NUMBER OF D/L CHANNELS
0 = 0 D/L Channels
2 = 2 D/L Channels
4 = 4 D/L Channels
6 = 6 D/L Channels (1) (2)

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating

CODE (See Code Table)

ENCODER/COMMUTATION
- = Without Encoder option
E = With Encoder option (3)

OPTIONAL REFERENCE SELECTION
0 = No “On Board Excitation”
A = 2-28 VRMS output
C = 115 VRMS fixed output

(1) Maximum Channel density is fixed at 8 LS/D and 6 D/L, which requires using the JP4 connector. See JP4 connector information (Table 7 & 7A).
(2) Selecting 6 channels of D/L with 0, 2 or 4 channels of L/D **only** will be configured to all channels residing on J1 connector. (See Table 6)
(3) Encoder/Commutation Options are for Measurement Channels only.

FOR OTHER VARIATIONS ON TOTAL CHANNEL COUNTS
(L/D AND D/L CONFIGURATIONS), PLEASE CONTACT FACTORY

Revision

Revision	Description of Change	Engineer	Date
1	Initial Release	GS	6/07/02
1.1	Swapped Interrupt Enable Bit Test #3	GS	6/12/02
1.2	For proper Soft Reset operation, 1μ < pulsewidth <=50ms.	GS	6/27/02
1.3	Correct Polarity in Diagrams for Principles of LVDT Operation	GS	6/28/02
1.4	Removed 0-13.5 volt reference option (from spec, and PN)	GS	7/18/02
1.5	Clarified Tables 7 and 7A for DS use only.	GS	7/26/02
1.6	Removed JP6-3 for Keying	GS	8/13/02
1.7	EXTERNAL +/- 12VDC: (JP6 & JP7)	GS	10/10/2
1.8	Corrects pinout in Table 7A	GS	11/1/2
1.9	Corrects pinout in Table 7A	GS	11/11/2
2.0	Address Range 174-1D0 moved to 19C-1F8. Also, Interrupt Enable now 1BC, Status 1C0	GS	1/20/3
2.1	Latch Output Functions Description, write 2 (not 1) to latch outputs	GS	1/21/3
2.2	Add less than 5ma per channel (not 1.2Va load). Line is eliminated as it is coved by the 140ma draw per 2 channel DL module	GS	9/5/3
2.3	New Address	KL	04/25/07