Four (4) D/S Channels (1.2 VA)

Single Speed or Two-Speed, Programmable
Multi-Speed Ratios: 2 to 255
D/S Rotation, Continuous Self-Test;
On-Board Programmable Reference Supply (Optional)
Both Commercial & Extended Temperature Ranges

FEATURES:

- 16 bit resolution
- 1 arc minute accuracy
- Continuous background bit testing for Reference and Signal loss detection
- Power-On Self-Test (POST)
- Automatically supports either 5V or 3.3V PCI bus
- 360 Hz to 10 kHz
- ON/OFF for D/S channels, redundant operation available (contact factory)
- I/O available via front panel, J2 or both
- Transformer isolated
- No adjustments or trimming required
- 2 or 4 channels available
- Part Number, S/N, Date Code & Revision in non-volatile memory

DESCRIPTION:

This single slot card contains **four separate transformer isolated Digital-to-Synchro/Resolver converters (1.2 VA), optional 5 VA reference, and extensive diagnostics. The (4) Stimulus channels include ON/OFF output capability, individual reference inputs are supplied for each channel, two-speed programmability, and rotation with start and stop angles.** The Stimulus channels offer short circuit protection and the ability to ground one of the outputs without effecting performance. External amplifiers can be added to drive up to 30 VA with a frequency range of 50 to 400 Hz. Each channel can be specified for a different voltage, frequency or resolution. To simplify logistics, Part number, S/N, Date code, & Rev. are located in permanent memory locations.

Major diagnostics are incorporated that offer substantial improvements to system reliability because the user is immediately alerted to channel malfunctions. This approach also reduces bus traffic because the *Status Registers* do not require constant polling. Power-On, Self-Test (POST) diagnostic can immediately initiate (D3) test.
See Programming Instructions for further details.

Two different tests (one on-line and one off-line) can be selected:

The (D2) Test initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the *commanded angle*. The status bits will be set to indicate an accuracy (0.05%) problem and the results can be read from *D/S Test Status Register*.

In addition, each Signal and Reference is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the Signal and Reference status registers.

The (D3) or POST test, (if enabled), starts a BIT Test that generates and tests 72 different angles, to a testing accuracy of 0.05°. Results can be read from Status Registers. External reference is required. Testing requires no external programming, and can be Initiated or terminated via the bus. CAUTION: Outputs are active during this test. Check connected loads for possible interaction.

(NOTE: ALL D/S TESTS REQUIRE THE OUTPUTS TO BE "ON" AND THAT A REFERENCE IS SUPPLIED.)

TABLE OF CONTENTS

This board can operate over a "C" or "E" operating temperature range (See part number). The "C" version (0°C to +70°C) uses standard high quality commercial semiconductors. The "E" version (-40°C to +85°C, used for severe environmental condition, uses high quality extended temperature semiconductors. Both sides of the board can be conformal coated (See P/N). All "E" boards are burned in for 24 hours and cycled from -40°C to +85°C.

SPECIFICATIONS:

D/S(R) CHANNELS (for each channel unless otherwise specified)

Resolution:	16 bits (.0055°)
Accuracy:	±1 arc minute (.0167°) at 1.2 VA. No load to full load
Two-Speed ratio:	Programmable from 2 to 255.
Rotation:	Programmable, Continuous or Start and Stop angles. 0 rps to ±13.5 rps with a resolution of 0.15°/sec. Stepping rate is 16 bits to 3.4 rps, then is automatically reduced to 14 bits up to 13.5 rps.
Output format:	Synchro or Resolver, (See part number), transformer isolated
Output voltage:	2-90 VL-L (See part number).
Output load:	1.2 VA max./Channel. Short circuit protected (5000 Ω reactive at 90 VL-L; Synchro, 90 Ω reactive at 11.8 Synchro, 110 Ω reactive at 11.8 VL-L Resolver)
Regulation:	5% max. No load to Full load
Reference voltage:	2-26VAC, 115VAC (See part number), transformer isolated.
Reference frequency:	360 Hz to 10 kHz (See part number). 47-60Hz for use with external amplifiers
Reference current:	1 ma max./Channel
Phase shift:	5° maximum between output and reference.
Settling time:	Less than 100 microseconds

REFERENCE SUPPLY: Optional. (See part number).

Voltage:	2-28Vrms programmable, or 115 Vrms fixed. Resolution 0.1 Vrms, Accuracy ±2%
Frequency:	360 Hz to 10 kHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 190mA RMS @ 2-28VAC, 45mA RMS @ 115VAC Note: Power is reduced linearly as the Reference Voltage decreases.

GENERAL SPECIFICATIONS:

Signal Logic Level:	Automatically supports either 5V or 3.3V PCI bus.	
Power:	See current requirement Table 1 below. Power supplies must be able to supply the peak power without current limiting.	
Temperature, operating:	"C" = 0°C to +70°C, "E" = -40°C to +85°C (See part number)	
Temperature, storage:	-55° C to +105° C	
Size:	3U, single slot 100mm x 20.3mm x 160mm deep	
Weight:	Board & heat sink less modules	6.0 oz. Max.
	D/S modules w/ transformers 2 Ch ea.	5.0 oz. Max.
	Reference module	1.8 oz. Max.

CURRENT REQUIREMENTS:

	±12Vdc	+5Vdc
Board – no Modules	15mA	460mA
Add per 2 Ch D/S Module	140mA	35mA
Add per 1.2 VA Load	125mA (400mA Peak)	
Reference Module		1A @ 5VA Load (3A Peak)

TABLE 1

MEMORY MAP

000	D/S Ch.1 Data	read/write
004	D/S Ch.2 Data	read/write
008	D/S Ch.3 Data	read/write
00C	D/S Ch.4 Data	read/write
020	Rotation rate, D/S Ch.1	read/write
024	Rotation rate, D/S Ch.2	read/write
028	Rotation rate, D/S Ch.3	read/write
02C	Rotation rate, D/S Ch.4	read/write
040	Stop angle Ch.1	read/write
044	Stop angle Ch.2	read/write
048	Stop angle Ch.3	read/write
04C	Stop angle Ch.4	read/write
060	Rotation Mode	read/write
064	Rotation, Initiate	write
068	Rotation, Stop	write
070	Wrap-around D/S Ch.1	read
074	Wrap-around D/S Ch.2	read
078	Wrap-around D/S Ch.3	read
07C	Wrap-around D/S Ch.4	read
090	Status, Signal	read
094	Status, Reference	read

TABLE 2

098	Status, Test	read
09C	Active channels	read/write
0A0	Interrupt Status	read
0A4	Interrupt Enable	read/write
0B0	Test (D2) verify	read/write
0B4	Test Enable	read/write
0B8	Power-On (POST)	read/write
0C0	Frequency (Ref. Supply)	read/write
0C4	Voltage (Ref. Supply)	read/write
0C8	Outputs ON/OFF	read/write
0D0	Ratio, D/S Ch.1/2	read/write
0D4	Ratio, D/S Ch.3/4	read/write
100	Watchdog timer	read/write
104	Soft reset	write
108	Part #	read
10C	Serial #	read
110	Date code	read
114	Rev level PCB	read
118	Rev level DSP	read
11C	Rev level Interface FPGA	read
120	Rev level FPGA	read
124	Save	read/write

TABLE 2 cont.

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data (angle)° Hi [1]	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Active channels	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
D/S outputs ON/OFF	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Rotation Mode	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Rotation, Initiate	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Rotation, Stop	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Rotation, Start/Stop	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Status, Test	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Status, Signal	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Status, Ref	X	X	X	X	X	X	X	X	X	X	X	X	DS4	DS3	DS2	DS1
Interrupt Enable/Status	X	X	X	X	X	X	X	X	X	X	X	X	X	TEST	REF	SIG

TABLE 3

Note 1 – Approximate values.

PROGRAMMING INSTRUCTIONS

At Power ON: or system reset, all parameters are restored to last saved setup and if POST is **enabled,** a D3 test is initiated.

Active Channels: Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel Register* ("1"=active; "0"=not used). **Omitting this step will produce errors on unused channels causing false alarms**; hence unused channels will set faults, i.e. status bits, interrupts, etc.

Write Angle – Single Speed:
For single-speed applications (Ratio=1), write a 16-bit integer (or 16-bit 2's compliment integer) to the corresponding channel *Data Register.* (ex. 330° = EAABh).
WORD = (Angle ÷ ($360/2^{16}$)).
Note: writing to an Input Angle Register will stop any rotation initiated on that channel

Ratio: Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Write Angle – Two-Speed:
In two-speed applications, the ratio will affect the fine speed output resolution. (Higher ratios result in lower resolutions at the output.) This occurs from multiplying the coarse angle by the ratio to achieve the fine angle output. This multiply reduces the overall resolution by increasing the weight of the LSB's. To compensate for this, the card allows for 24-bit resolution for the higher ratios. This feature is transparent and automatic to the user and will regain the resolution needed in higher ratio systems.

When 16 bit resolution is sufficient, the angle can be represented by first writing the integer 0 to the even channel of the pair *Data Register,* then a 16-bit integer (or 16-bit 2's compliment integer) to the odd channel of the pair (coarse speed) *Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. Note: Integer 0 only needs to be written to the even channel once to initialize the even channel register. Subsequently, only writes to the odd channel are necessary.

Odd Channel	Even Channel
16 Bits	0

16 bit integer = Angle / ($360/2^{16}$); Fine Speed ≡ Angle * Ratio / ($360/2^{16}$)

Ex1. For a ratio of 255, the fine speed output would have a resolution of 1.4008°.
Thus, for every 0.00549° of shaft angle, the fine output will change in 1.4008° increments.

When 24 bit resolution is desired, the angle can be represented as a 24-bit integer (or 24-bit 2's compliment integer) by first writing the lower 8-bits to the upper byte of the even channel of the pair *Data Register*, then the upper 16-bits to the odd channel of the pair (coarse speed) *Data Register*. The card will set the angle of second channel output (fine speed), to the coarse angle multiplied by the ratio. The channel pairs are defined as Ch1&2, Ch3&4, Ch5&6 and Ch7&8.

Odd Channel	Even Channel	
16 Bits	8 Bits	X

24 bit integer = Angle / ($360/2^{24}$); Fine Speed ≡ Angle * Ratio / ($360/2^{24}$)

Ex1. For a ratio of 255, the fine speed output would have a resolution of 0.00547°.
Thus, for every 0.000021458° of shaft angle, the fine output will change in 0.00547° increments.

Note: Writing to an input angle register will stop any rotation initiated on that channel.

Two-Speed Connectivity: In two-speed D/S applications, the odd channel output of the pair provides the single speed (coarse) information. The even channel output of the pair provides the N-speed (multi-speed, fine) information. The pairs are defined as: CH1 & 2 & CH3 & 4.

Outputs ON/OFF: Set the bit corresponding to each channel to be turned on, to "1" in the *Output On/Off Register*. To turn OFF a channel, set corresponding bit to "0". Default is OFF.

Read Wrap-Around Angles: Wrap-around angles are read from the *D/S Wrap-around Registers*. Each enabled D/S channel is measured prior to the transformer output and can be read from the corresponding *D/S Wrap-around Register*. The generated result is a 16-bit binary word (or 16-bit 2's compliment word). The data is available at any time.

Rotation Rate: Write a 2's compliment number representing the desired rotation rate, to the corresponding *Rotation Rate Register*. LSB = 0.15°/sec.

Ex: 12 RPS = (12 x (360°/0.15°) = 28800 (7080h), -12 RPS = (-12 x (360°/0.15°) = -28800 (8F80h).
Stepping rate is 16 bits (0.0055°) for up to 3.4 RPS, then linearly decreases to 14 bits (0.022°) at 13.5 RPS.

Rotation Mode, Continuous or Start/Stop: For continuous rotation, set the corresponding channel bits to "0" in the *Rotation Mode Register*. For rotation to cease at a designated stop angle, set the bit to "1".

Stop Angles: Write the desired stop angle to appropriate channel *Stop Angle Register*. After a channel reaches the stop angle, it will stop rotating and remain at that angle until a new input angle is set. If rotation is initiated again, the angle will start rotating from the present angle.

Initiate Rotation: First set the *Rotation Rate* and *Rotation Mode Register* for each channel that is to rotate. Then, to start rotation for those channels, set the corresponding channel bit to a "1" in the *Rotation Initiate Register*.

Stop Rotation: Set the corresponding bit, for each channel to be stopped, to a "1" in the *Rotation Stop Register*. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated.

Rotation Completed: (not implemented - consult factory) *Read the Rotation Completed Register. Each bit corresponds to a given channel. A "1" = rotation completed, "0"=rotation in process.*

Power-On Self-Test (POST): The unit will initiate the D3 Test on Power-On, if POST is enabled and saved. Enable by writing "1" or Disable by writing "0" to *POST Register* and then save setup.

D2 Test Enable: Writing "1" to the D2 bit of the *Test Enable Register* initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the commanded angle. The status bits will be set to indicate an accuracy problem and the results can be read from the *Test Status Register* within 2 seconds and if enabled, an interrupt will be generated (See *Interrupt Register*. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Outputs must be ON and Reference supplied for test to function. Card will write 55h (every 2 seconds) to the *Test (D2) Verify Register* when D2 is enabled. User can periodically clear to 00h and then read the *Test (D2) Verify Register* again, after 2 seconds, to verify that BIT Testing is activated. This test continuously sequences between the four channels on the card with each output being measured for approx. 180 mSec. If the measured angle has an error greater the 0.05º, a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

In addition, each D/S Reference input and signal output is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Reference Status Registers*.

D3 Test Enable: Writing "1" to the D3 bit of the *Test Enable Register* initiates a BIT Test that generates and tests 72 different angles to an accuracy of 0.05°. External reference is required and outputs must be ON. The *Test* Status bits will be set to indicate an accuracy problem. Results are available in the *Test Status Registers* and if enabled, an interrupt will be generated (See *Interrupt Register*). Test cycle takes about 30 seconds and the D3 bit

changes from “1” to “0” when test is complete. The testing requires no external programming, and can be terminated at any time by writing a “0” to the D3 bit of the *Test Enable Register*.
CAUTION: Outputs must be ON and Reference supplied during this test and is therefore active. Check connected loads for possible interaction.

Status, Test: Check the corresponding bit of the *Test Status Register* for status of BIT Testing for each active channel. A ”1” means Accuracy OK; “0” failed. Channels that are inactive are also set to “0”. (test cycle takes 2 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register.

Status, Ref: Check the corresponding bit of the *Reference Status Register* for status of the reference input for each active channel. A ”1” means Reference ON, “0” means Reference Loss on active channels. Channels that are inactive are also set to “0”. (Reference loss is detected after 2 seconds). Reference monitoring is always enabled. Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

Status, Sig: Check the corresponding bit of the *Signal Status Register* for status of the output signals for each active channel. A "1" means Signal is valid, “0” means Signal loss. Channels that are inactive are also set to “0”. (Signal loss is detected after 2 seconds). Signal monitoring is always enabled. Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

Power On Reset or System Reset: All parameters are restored to last saved setup and, if POST was previously enabled in last setup, a D3 Test will be initiated. A power on automatic calibration test is run and completes in approximately 30 seconds.

Save Setup: Writing 5555h to the *Save Register* will save the current setup. This location will automatically clear to 0000h when save is completed (within 5 seconds). When save is elected, all parameters are saved. However, any parameter can be changed at any time. Saving is optional. If not saved, reenter parameters at each Power-On. To restore factory shipped parameters, write AAAAh to the *Save Register*, followed by System Reset. Note: After a SAVE or RESTORE, poll the *Save Register* and **do not perform any operation until word is at 0000h.**

Interrupt Registers: Interrupts can be enabled to relay specific problems/failures detected by the card. The problem/failures that generate these interrupts are:

D/S Signal Loss, D/S Reference Loss & D/S Test Accuracy Error

Each external interrupt can be enabled individually. This is accomplished by writing a “1” to the bit corresponding to desired interrupts to the *Interrupt Enable Register* and a “0” to disable those interrupts not used.

Interrupt Status Registers: When an interrupt is initiated via a problem/failure, the *Interrupt Status Register* can be interrogated by a read to identify, which interrupt had occurred. Refer to Table 3. Register is latched when interrupt is generated and unlatched when read.

Note: This register is typically read and cleared by the device driver. Subsequent readings of this register will give clear status.

Optional Reference Supply: For frequency, write a 16-bit integer to the *Frequency Ref Supply Register*. (Ex: 400 Hz = 0190h) with LSB= 1Hz. For voltage, write a 16-bit integer to the *Voltage Ref Supply Register* (Ex: 26Vrms =0104h) with LSB=0.1Vrms. It is recommended that the user program the required frequency before setting the output voltage.

Soft Reset: Write an integer "1" to *Soft Reset Register*, then clear to 0 before 50ms elapses. **CAUTION: Register is level sensitive and for proper card operation, the logic level "1", or pulsewidth, must be <= 50ms**. Considering minimum and maximum, 1 µs < pulse width <= 50ms. Processor reboots in about 400 ms, after which calibration procedures begin. This function is equivalent to a power-on reset.

Watchdog Timer: This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number: Read as a 16-bit binary word from the *Serial Number Regi*ster. Serial number of purchased board.

Date Code: Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week)

Rev Levels: There are a total of 4 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Rev level PCB Rev level D/S DSP Rev level D/S FPGA Rev level Interface FPGA

LED's & µTEST CONNECTORS: The board contains two green LED's that are for factory use only. The two-miniature test connectors are used during download programming data. Do not interface to these two connectors unless factory instructed.

SOFTWARE - PCI PROGRAMMING:

This section provides programmers the information needed for developing drivers other than those supplied.
The following information resides in the PCI configuration registers:

Device ID	= 7511	(hex)
Vendor ID	= 15AC	(hex)
Rev	= 01	(hex)
Subsystem ID	= 000115AC	(hex)

Base Address = Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information.
Required Address space = 1K for each card.

I/O CONNECTOR PINOUTS

J2Connector (REAR)

J2D-20	**RLO-OUT**	**J2E-18**	**S4-CH4**	J2F-22	GND
J2D-21	**RHI-OUT**	**J2E-21**	**S2-CH4**	J2F-21	GND
J2D-20	N/C	**J2E-20**	**S3-CH4**	J2F-20	GND
J2D-19	N/C	**J2E-19**	**S1-CH4**	J2F-19	GND
J2D-18	**RLO-CH4**	J2E-18	N/C	J2F-18	GND
J2D-17	**RHI-CH4**	J2E-17	N/C	J2F-17	GND
J2D-16	N/C	**J2E-16**	**S4-CH3**	J2F-16	GND
J2D-15	N/C	**J2E-15**	**S2-CH3**	J2F-15	GND
J2D-14	N/C	**J2E-14**	**S3-CH3**	J2F-14	GND
J2D-13	N/C	**J2E-13**	**S1-CH3**	J2F-13	GND
J2D-12	**RLO-CH3**	J2E-12	N/C	J2F-12	GND
J2D-11	**RHI-CH3**	J2E-11	N/C	J2F-11	GND
J2D-10	N/C	**J2E-10**	**S4-CH2**	J2F-10	GND
J2D-9	N/C	**J2E-9**	**S2-CH2**	J2F-9	GND
J2D-8	N/C	**J2E-8**	**S3-CH2**	J2F-8	GND
J2D-7	N/C	**J2E-7**	**S1-CH2**	J2F-7	GND
J2D-6	**RLO-CH2**	J2E-6	N/C	J2F-6	GND
J2D-5	**RHI-CH2**	J2E-5	N/C	J2F-5	GND
J2D-4	N/C	**J2E-4**	**S4-CH1**	J2F-4	GND
J2D-3	N/C	**J2E-3**	**S2-CH1**	J2F-3	GND
J2D-2	**RLO-CH1**	**J2E-2**	**S3-CH1**	J2F-2	GND
J2D-1	**RHI-CH1**	**J2E-1**	**S1-CH1**	J2F-1	GND

TABLE 4
N/C - denotes no connections

As of June 1, 2004 S4-CH4 and RLO-OUT has been moved from E22 and D22 to E18 and D20 respectively to support cPCI Geographical Addressing.

P1 - Optional Front Connector; see P/N DC37P; Mate: DC37S

Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation
35	S1 DS 1	12	S1 DS 2	25	S1 DS 3	20	S1 DS 4	19	Ref Lo Out
16	S2 DS 1	30	S2 DS 2	8	S2 DS 3	21	S2 DS 4	37	Ref Hi Out
17	S3 DS 1	31	S3 DS 2	7	S3 DS 3	1	S3 DS 4		
34	S4 DS 1	11	S4 DS 2	26	S4 DS 3	2	S4 DS 4		
15	RLo DS 1	10	RLo DS 2	6	RLo DS 3	3	RLo DS 4		
33	RHi DS 1	29	RHi DS 2	24	RHi DS 3	22	RHi DS 4		

TABLE 5
S4 pins used only with Resolvers.

CODE TABLE

Code	Output (VL-L)	Ref (Vrms)	Freq. (Hz)	Load	Comments
01	11.8	26	400	1.2 VA	
02	90	115	400	1.2 VA	

See code list addendum for descriptions of code 50 and above.

TABLE 6

PART NUMBER DESIGNATION

75DS1- XX X X X X - XX

TOTAL NUMBER OF CHANNELS
02 – 2 D/S Channels
04 – 4 D/S Channels

CODE (See Code Table)

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

OPTIONAL REFERENCE SELECTION
0 = No "On Board Reference"
A = 2-28 VRMS output
C = 115 VRMS fixed output

FORMAT
S = Synchro
R = Resolver
M = Mixed (See Code Table)

MECHANICAL
F = Front Panel I/O only
B = Front Panel I/O and J2 I/O
P = J2 I/O only
Note: J2 connections can not be used for Analog signals in a PXI chassis. Analog Outputs must be via the front panel I/O only (F).

REVISION PAGE:

Revision	Description of Change	Engineer	Date
Rev 1.5	Orignal 3 page document	FH	09/24/01
Rev 2.0	Added header and footer; Updated specifications; Added descriptions for D/S section and additional functions; Assigned numbering to tables; Added memory and register map. Added connector I/O tables and updated code table.	WG/BC	10/02/01
Rev 2.1	Added Revision sheet.	BC	10/11/01
Rev 2.2	Added date to revision sheet	BC	10/22/01
Rev 2.3	Removed reference made to "common references" in description section; Added column for engineer to revision page; Modified connector tables.	FH/BC	10/23/01
Rev 2.4	Clarified Reference supply specification; corrected board weight w/heat sink; Updated optional reference selection in part number description.	FH	10/25/01
Rev 2.5	Removed "24 bit combined" from bullet on title page; Adjusted right margin on title page; Split up programming instructions and memory map headings. Removed reference made to "can be specified by adding "W" to P/N" from pg. 2.; Added PCI programming section; Corrected code 3 of the code table; Updated description of two-speed operation; Modified 'M' to 'E' temp range. Deleted Rotation Completed command.	FH/PF/BC	11/21/01
Rev 2.6	Register Map D/S Channel Data is read/write	GS	12/20/01
Rev 2.7	See code list addendum for descriptions of code 50 and above. Removed D/S Ratio. Part Number: contact factory for other temperature req'ts. Moved 2-Spd Conn. Automatically supports either 5V or 3.3V logic levels.	GS	02/04/02
2.8	Changed code 1 & 2 to "01" & "02"	GS	05/08/02
2.9	For proper Soft Reset operation, 1µ < pulsewidth <=50ms.	GS	6/27/02
3.0	Removed 2-13.5 volt reference option (from spec, and PN)	GS	6/28/02
3.1	Added D3/POST test description to page 1. Revealed revision control sheet.	GS	2/4/3
3.2	Adds address 94 to Spec (was not viewable)	GS	3/10/4
3.3	Conducted cooled versions available. As of June 1, 2004 S4-CH4 and RLO-OUT has been moved from E22 and D22 to E18 and D20 respectively to support cPCI Geographical Addressing	GS	7/7/4
3.4	Adds Save register description	GS	1/27/5
3.5	Removes Wedgelock option from PN. Conduction cooled version is NOT available	GS	4/19/5
3.6	Changed Address	DD	05/07/07
A	Initial release to agile - reformatted to newer format, revised accuracy spec.	FR	04/1//2011